# INVESTOR DAY PRESENTATION

June 18, 2026

# Safe Harbor Statement

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward-looking statements, which are found in various places throughout the presentation, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward-looking statements, although not all forward-looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward-looking statements. While these forward-looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward-looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 and other global pandemics and the associated adverse impacts on the global economy, financial markets, global supply chains and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; consolidation activity and industry alliances in the semiconductor industry that may result in further increased customer concentration, inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, conflict minerals regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region where we have a substantial portion of our production facilities; potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel, including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers.

In addition, the United States and other countries have recently levied tariffs and taxes on certain goods and could significantly increase or impose new tariffs on a broad array of goods. They have imposed, and may continue to impose, new trade restrictions and export regulations. Increased or new tariffs and additional taxes, including any retaliatory measures, trade restrictions and export regulations, could negatively impact end-user demand and customer investment in semiconductor equipment, increase Besi’s supply chain complexity and manufacturing costs, decrease margins, reduce the competitiveness of our products or restrict our ability to sell products, provide services or purchase necessary equipment and supplies. Any or all of the foregoing factor could have a material and adverse effect on our business, results of operations or financial condition. In addition, investors should consider those additional risk factors set forth in Besi's annual report for the year ended December 31, 2025 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.

# Agenda

| | | | |
|---|---|---|---|
| I. | Strategic Overview | Richard Blickman | 13.00 – 13.20 |
| II. | Market Trends | Chris Scanlan | 13.20 – 13.50 |
| III. | Wafer Level Assembly | Peter Wiedner | 13.50 – 14.15 |
| | Break | | 14.15 – 14.30 |
| IV. | Mainstream Die Attach | Christoph Scheiring | 14.30 – 14.45 |
| V. | Summary | Richard Blickman | 14.45 – 15.00 |
| VI. | Q&A | Besi Team | 15.00 – 16.00 |

# I. STRATEGIC OVERVIEW
## Richard Blickman
## CEO

# Executive Summary

## Significant Progress Achieved on Long-Term Plan Realization

- Overall market conditions have improved significantly. 50%+ assembly equipment growth anticipated 2025-2028
- Market share leadership increasing
  - Expect to grow ~3x more rapidly than overall assembly equipment market through 2030
- Besi's business profile has significantly changed versus prior cycle
  - AI demand is primary driver of Besi's order growth starting Q3-25
  - Since Q2 2025, orders up 71% versus comparable 9 month period
- Improving gross and net margins, disciplined expense management and operating leverage aid realization of long-term profit goals
- Hybrid bonding adoption and use cases increasing in logic, memory, CPO and consumer

## Three revenue streams emerging each with attractive growth profiles

- 2.5D assembly equipment growth expanding due to strong data center and photonics demand by Asian subcontractors for current AI applications
- 3D assembly gaining traction for next gen AI use cases and More than Moore architectures
- Traditional mainstream improving as semiconductor inventories move from surplus to deficit conditions and unit growth now above long term trendline

# Executive Summary

## Multiple drivers converging to accelerate hybrid bonding growth

- Growth anticipated in 2027/2028 as customer road maps converge
  - In logic: AMD, Intel and Apple already in production. On roadmap of Broadcom ASIC accelerator and Nvidia Feynman
  - In memory: HBM 4e insertion point
  - In CPO: TSM COUPE in production with multiple customers (Nvidia and Marvell)

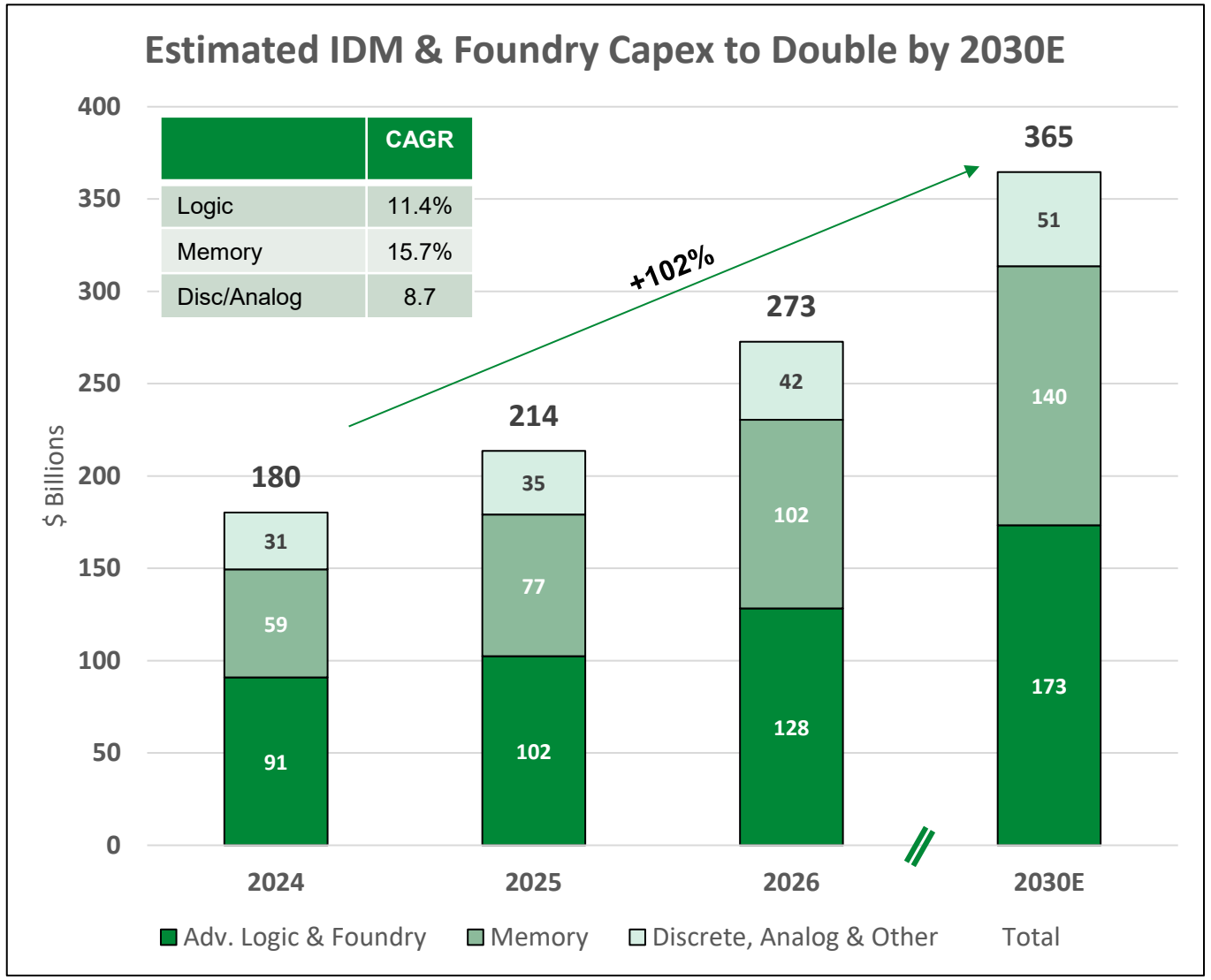
## Adjusting operating model in alignment with growth potential

- Increasing supply chain capabilities to accommodate production of 35 HB/month
- Building new VNM assembly facility to free up advanced packaging capacity in MY
- Increasing service/support capabilities in Taiwan, Korea and US

## Increasing 2030 targets

- Upping revenue target to between € 1.7 - € 2.2 billion (~+15% versus last Investor Day)
- Increasing low end of operating margin range
- All other targets unchanged versus last Investor Day

# Overall WFE Outlook Improving Due to AI Infrastructure Build




Source: TechInsights, June 2026

## AI Buildout Has Caused New Multi-year WFE Capex Cycle

**"It will be a long time before we can meet customer demand"** (C.C. Wei. *June 2026)*

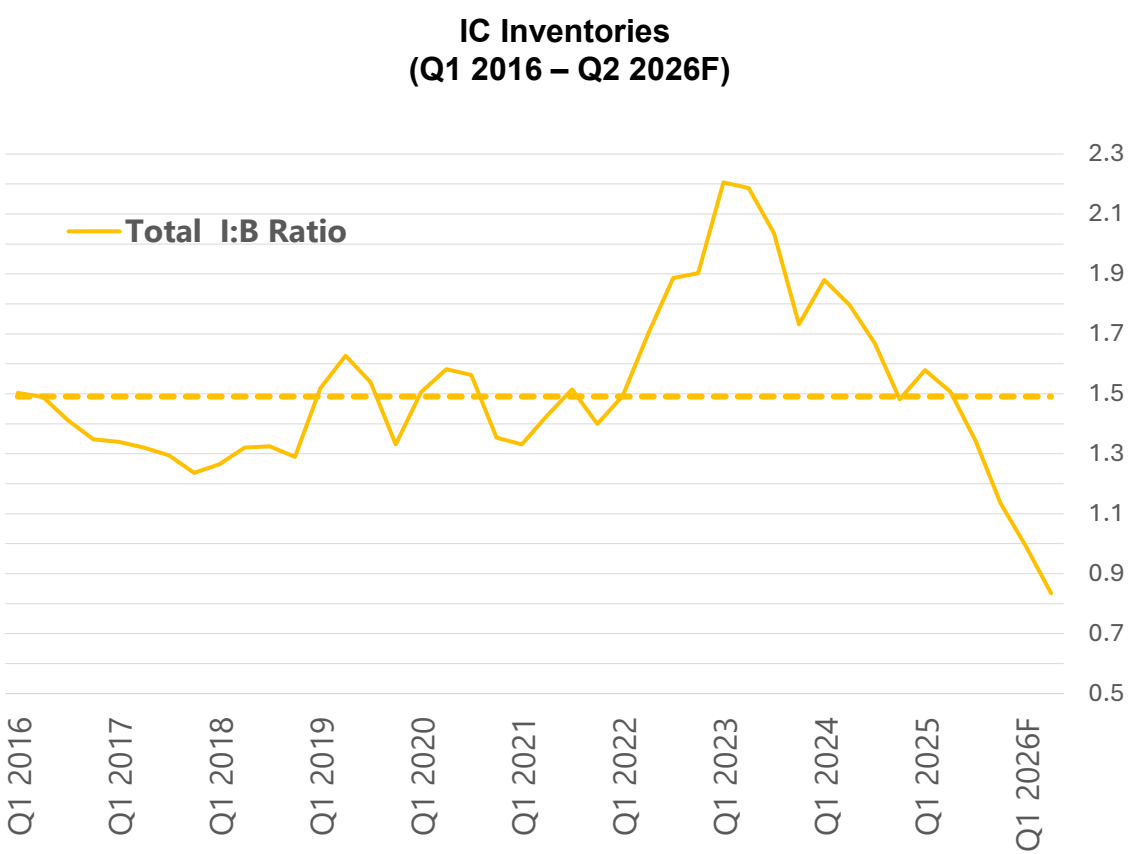
**"[Customers] are placing their orders early…Our visibility runs all the way to 2028 right now."** (H. Tan. June 2026)

**"Our largest customers are providing rolling 8-quarter forecasts so we can prepare...for their ramps"** (G.Dickerson. May 2026)

**"We have supply for very, very robust growth, but we're still supply constrained."** (J. Huang. June 2026)

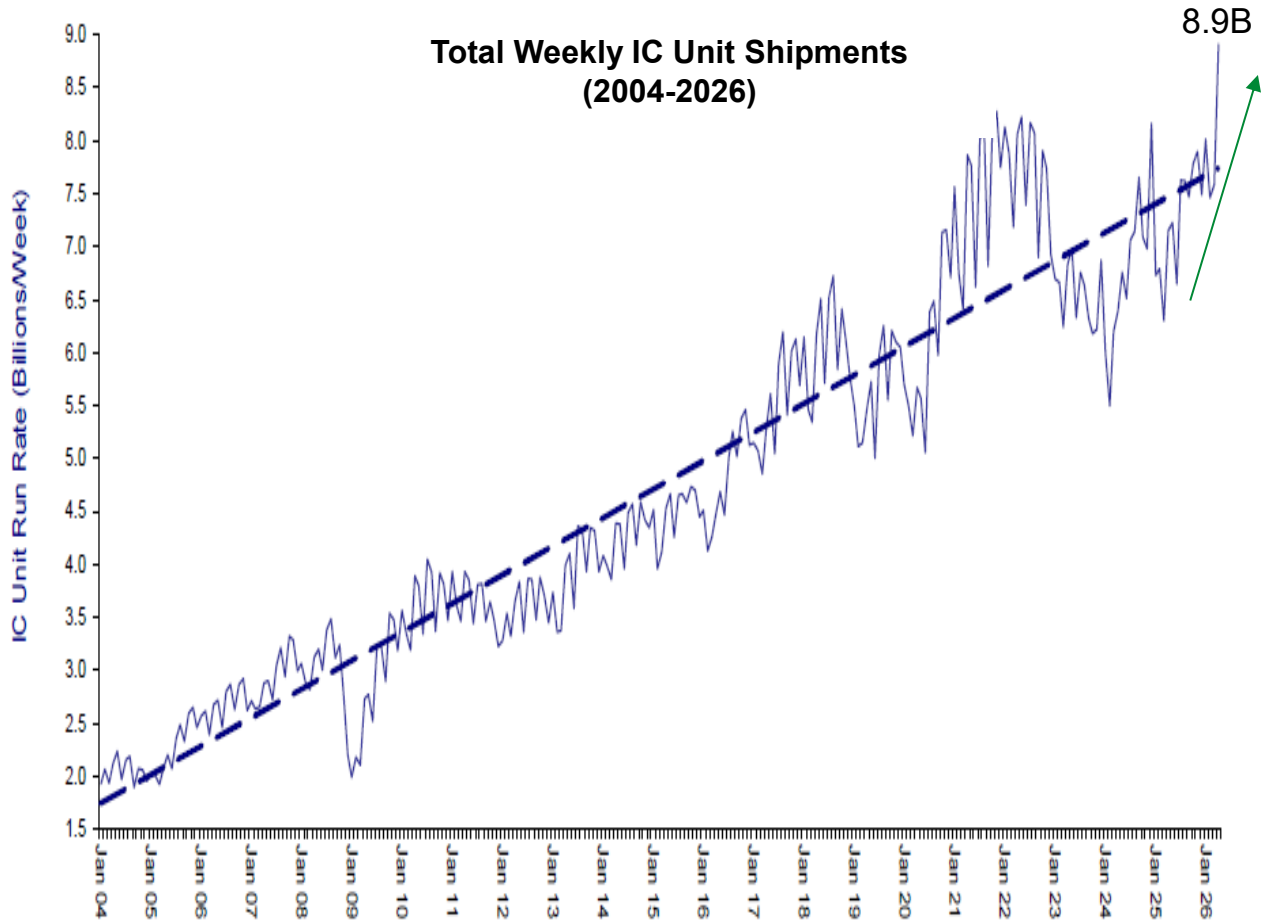
# Similarly, Semiconductor Inventory Levels Have Moved from Surplus to Deficit Conditions and Unit Growth Now Above Long Term Trendline

## Semi Inventory/Bookings Ratio Indicates Order Growth Outpacing Inventory Levels



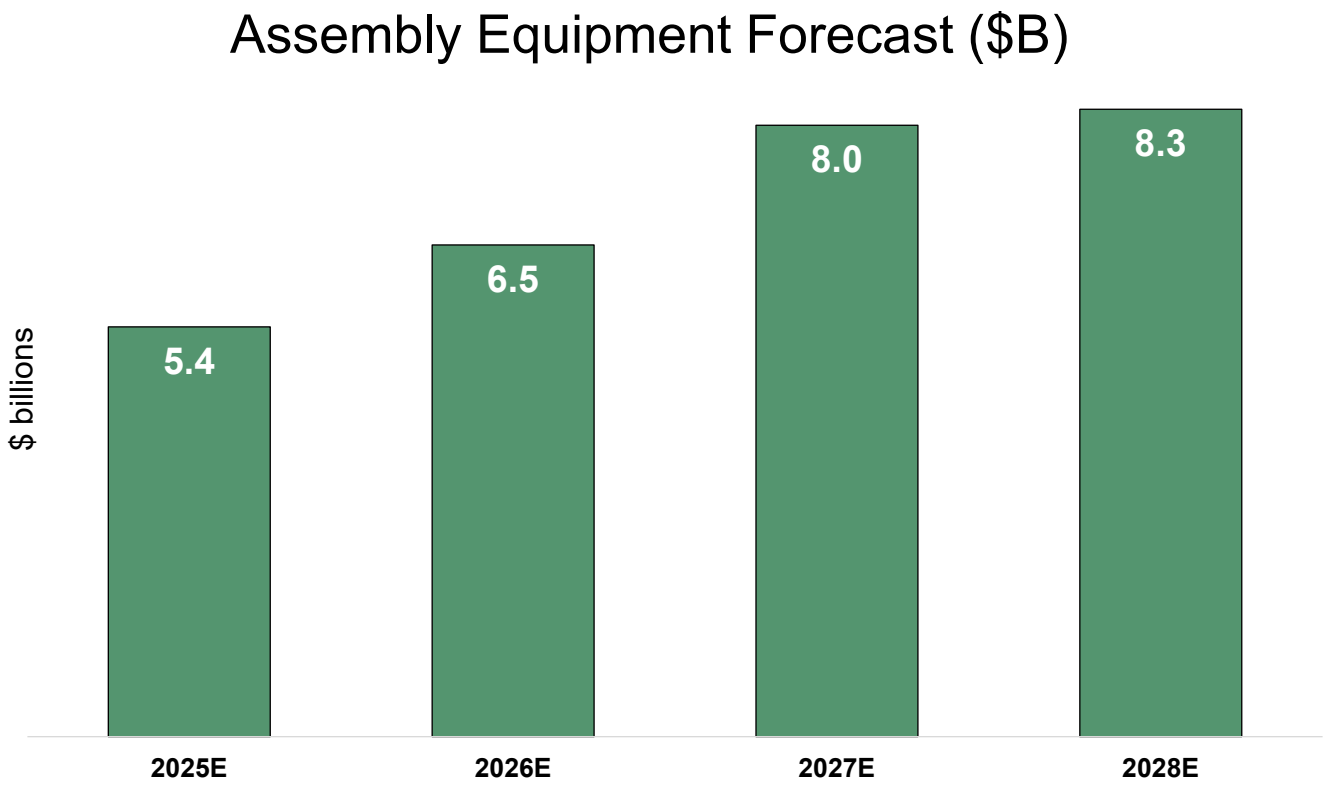

Source: TechInsights, June 2026

## Favorable IC Unit Growth Trends




Source: Future Horizons, June 2026

# Assembly Equipment Growth Also Expected to Accelerate




**TechInsights forecasts renewed assembly growth**

- **20% increase anticipated in 2026**
- **53% increase expected 2025-2028**
  - Expansion of AI/use cases
  - Recovery of mainstream applications
  - New fabs coming online
- Broad based advanced packaging growth expected

**Besi expects to grow ~3x more rapidly than projected assembly market growth as per TechInsights**

Source: TechInsights, June 2026. Assembly equipment revenue excludes service revenue

# Many New Advanced Packaging Fabs Planned

## ~$125B Investment Planned or In Progress

| Packaging Fab Projects | # Projects | Cost ($B) |
|---|---|---|
| USA | 7 | 33 |
| Taiwan | 6 | 30 |
| Korea | 3 | 26 |
| India | 3 | 10 |
| Singapore | 1 | 7 |
| China | 7 | 6 |
| Europe | 5 | 5 |
| Vietnam | 2 | 5 |
| Malaysia | 3 | 3 |

Source: TechInsights, Besi estimates, June 2026

- **Planned spending up 25% vs. last Investor Day**
  - Increased number of projects in US, Taiwan and Korea
  - CoWoS and HBM packaging expansion

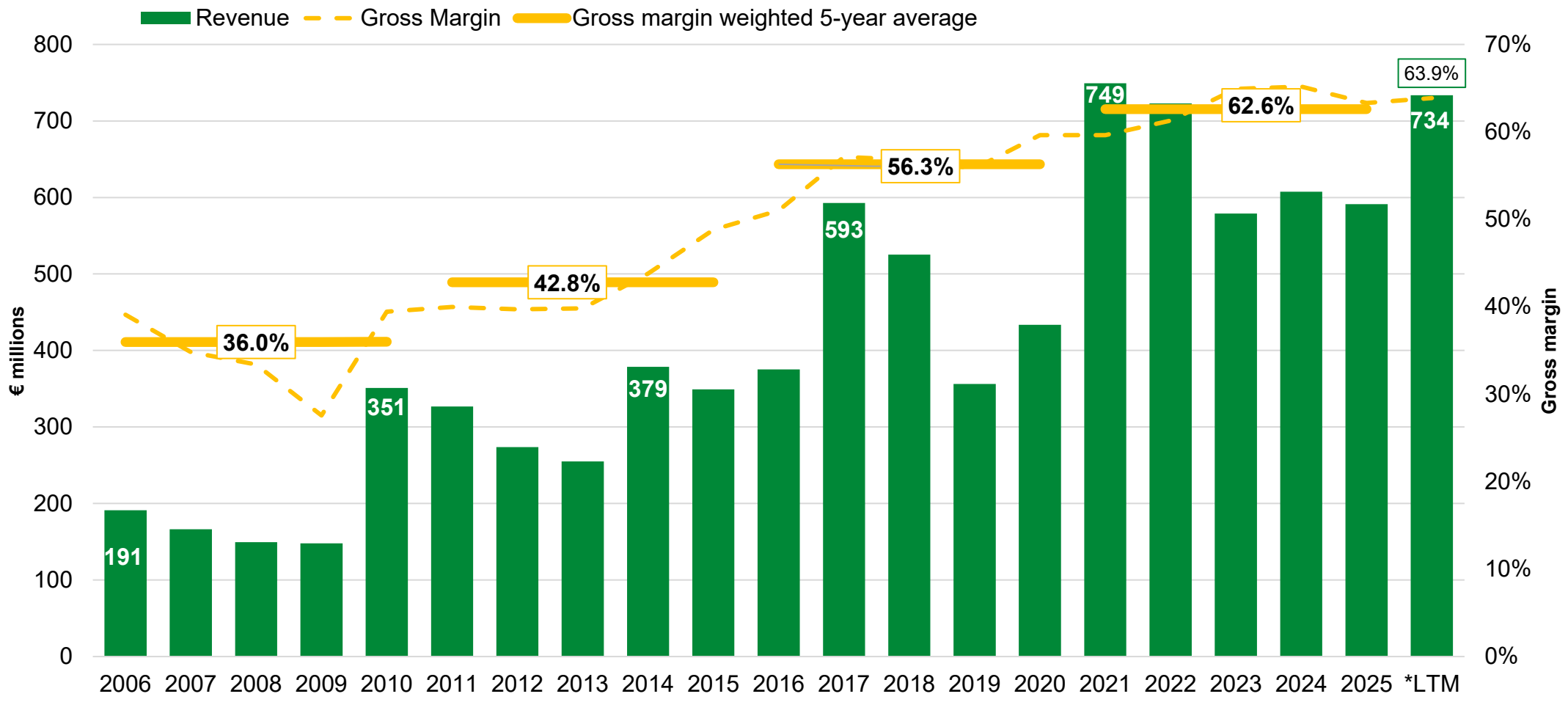
Amkor accelerates US expansion with Arizona investment and closer alignment with TSMC

ASE raises 2026 capex to record US$8.5 billion on strong advanced packaging demand

Packaging and testing cluster expected to emerge as TSMC Arizona GigaFab expands

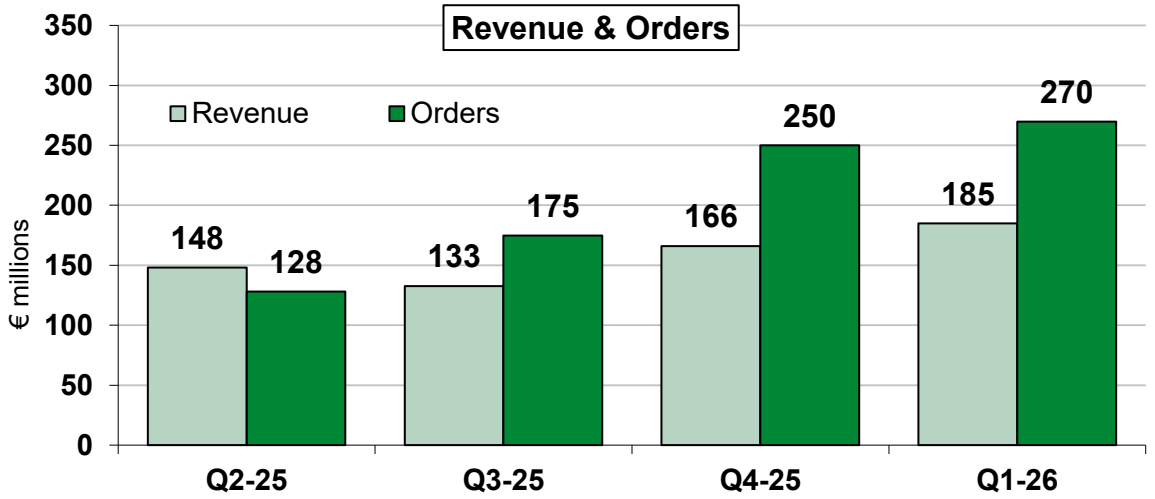
**SK Hynix to invest $13 billion in new plant amid memory chip shortage**

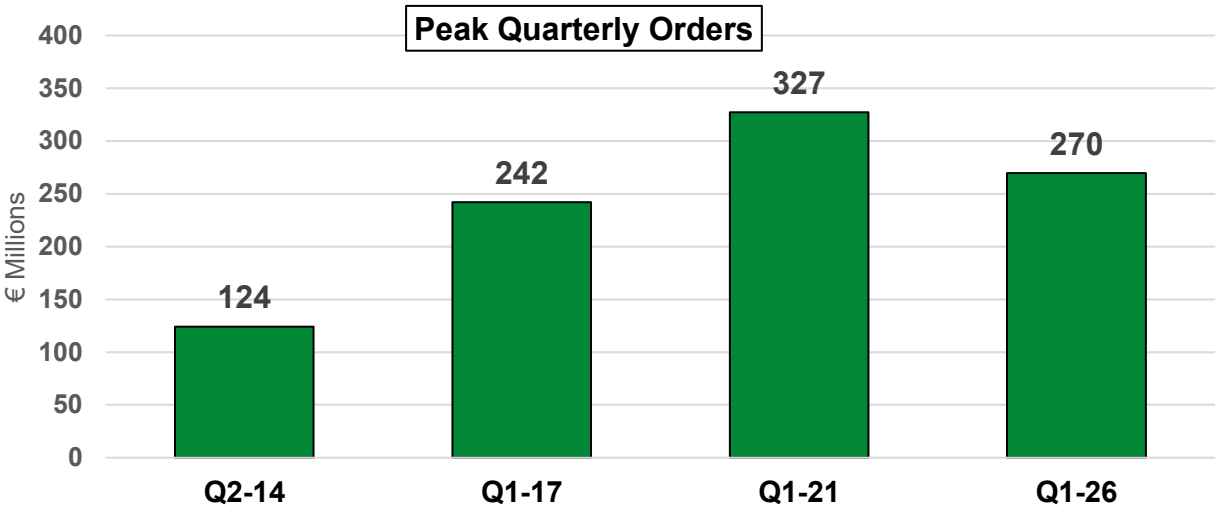
# New Besi Upcycle Began in H2-25

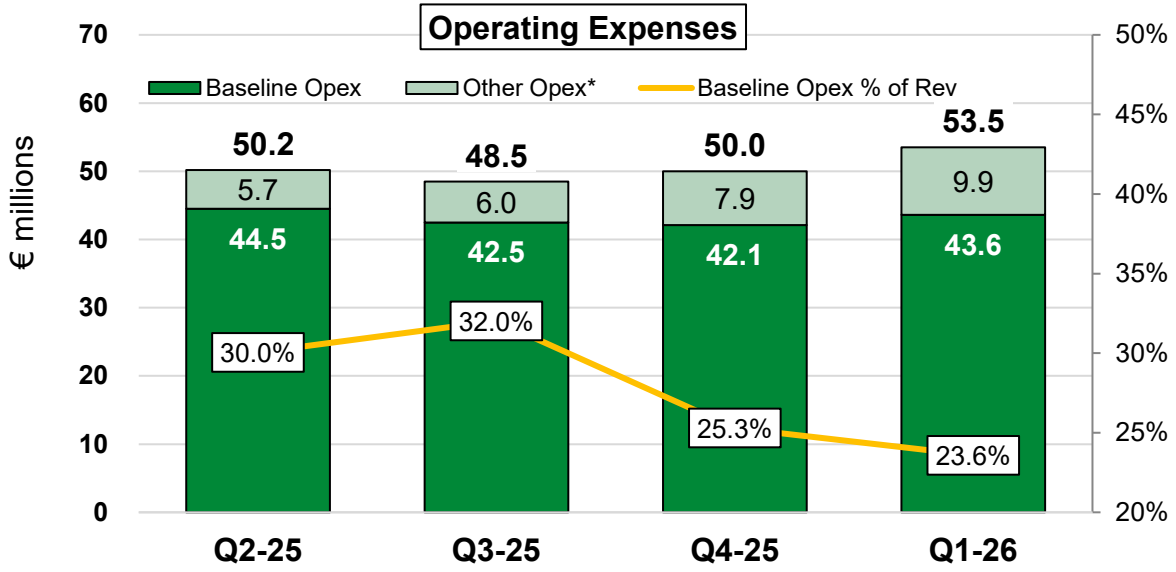


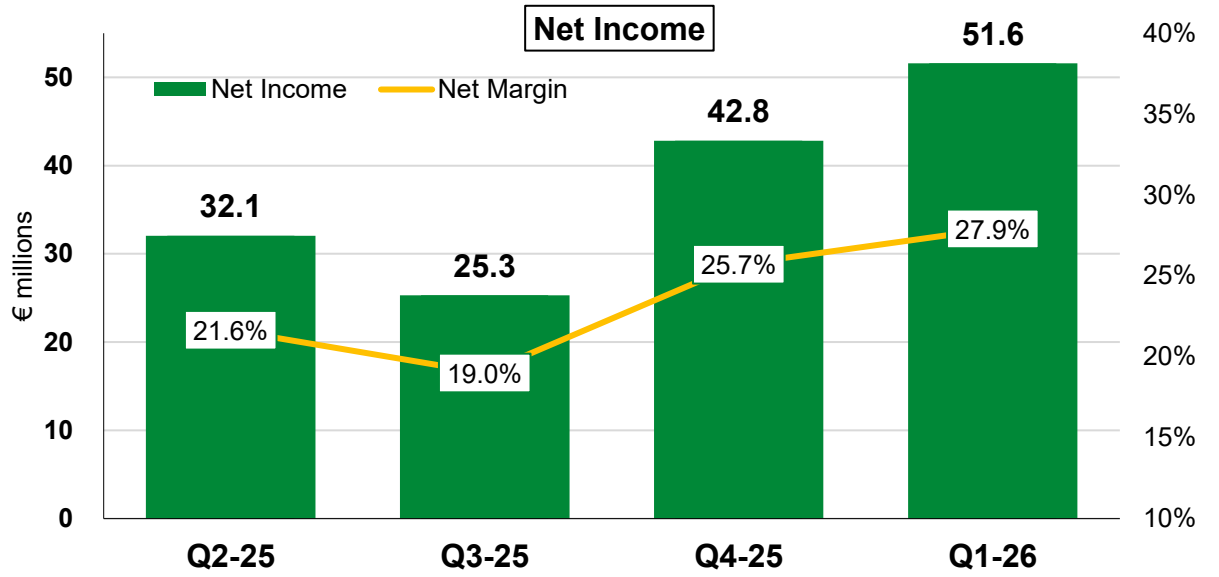

* At midpoint of Q2-26 guidance

# Revenue, Orders and Profitability Have Accelerated Since Q2-25

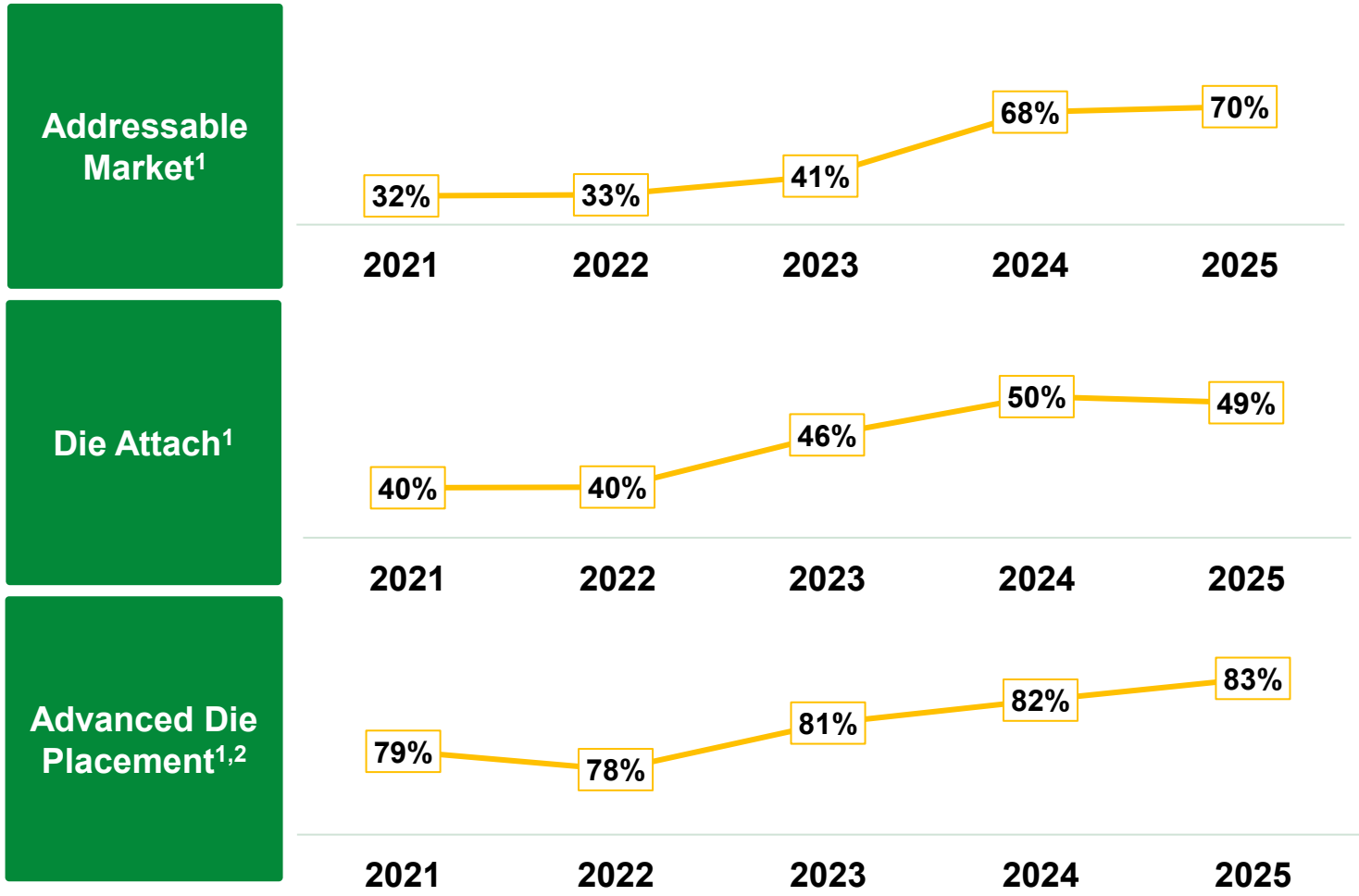


# Well Positioned With Leading Market Shares In Its Addressable Markets




Source: TechInsights, May 2026

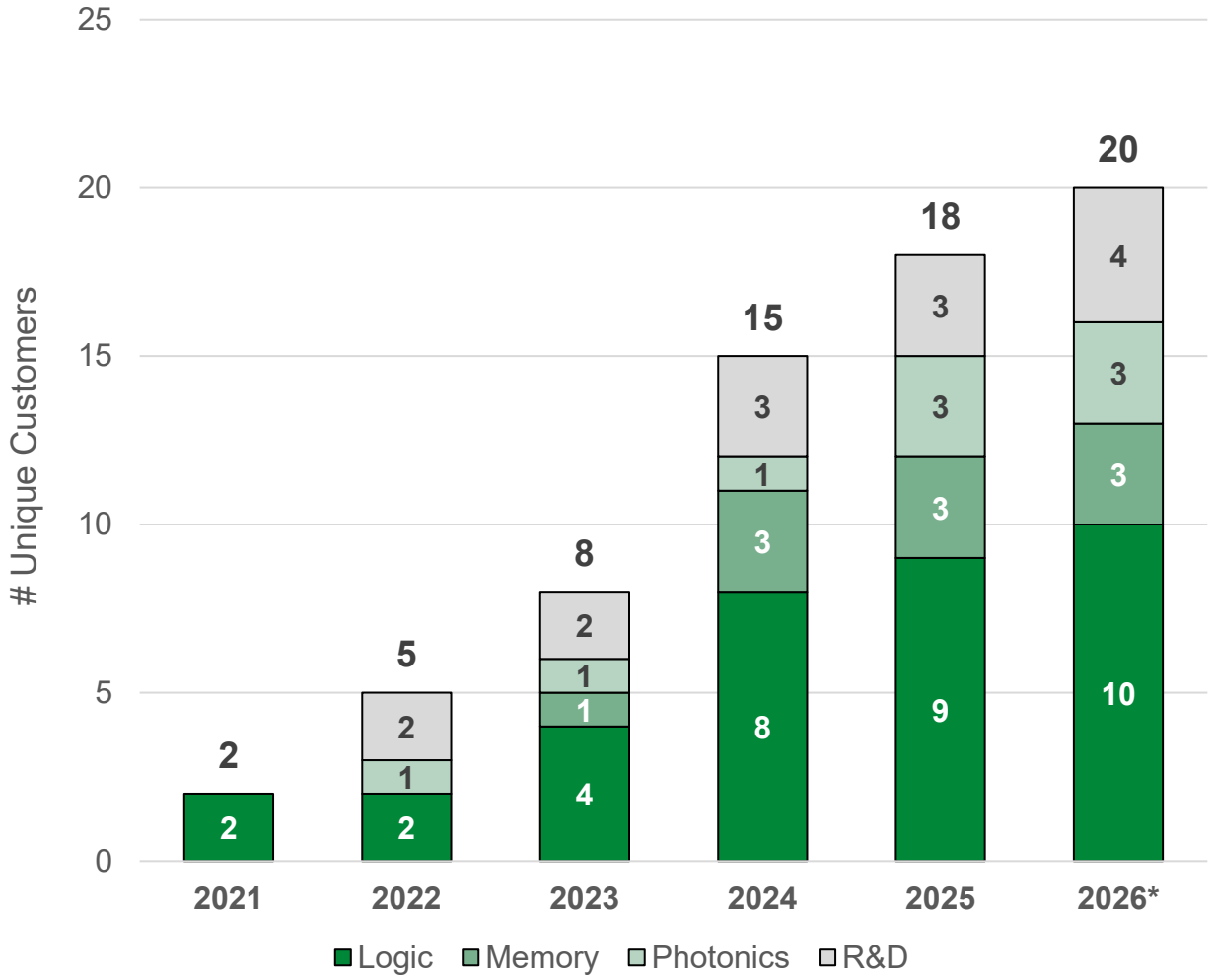
1) Excludes TCB, wire bonding, dicing, and other
2) Advanced die placement defined as < 7 micron accuracy per TechInsights

# Long Term Outlook Enhanced By Increased Hybrid Bonding Use Cases and Products in the News

| | |
|---|---|
| tsmc | "TSMC says COUPE platform set for production as Samsung outlines Silicon Photonics push" *Digitimes Asia. April 2026*<br>"Taiwan's TSMC advanced packaging fabs on schedule" TSMC is expanding its advanced packaging capacity, especially SoIC hybrid bonding, which enables 3D stacking. *Taiwan News. March 2026* |
| BROADCOM | "Semiconductor Equipment's Next Gold Mine" Broadcom XDSiP 3.5D platform's core feature is hybrid copper bonding *36Kr Europe. March 2026*<br>"Broadcom paves path for the 200T AI Era" Broadcom highlights optical roadmap, including co-packaged optics and photonics enabled scaling for future AI networks. *Broadcom. March 2026* |
| SK hynix | "Hybrid bonding expands from logic to memory: SK Hynix, Applied Materials, Besi drive co-optimization to scale next-gen HBM" *Counterpoint. April 2026*<br>"SK Hynix eyes hybrid bonding for HBM5 launch by 2029" *Counterpoint. April 2026* |
| NVIDIA | "NVIDIA Rubin Ultra and Feynman reportedly to boost TSMC SoIC; Besi, Applied Materials, TEL to benefit" *Trendforce. March 2026*<br>"NVIDIA Feynman GPU gets 3D die-stacking, custom HBM & Next gen Rosa CPU" *Wccftech. March 2026* |
| BROADCOM FUJITSU | "Fujitsu is utilizing Broadcom's proprietary 3.5D eXtreme Dimension System in Package (XDSiP) platform to build the chip". Broadcom's tech flips the dies to stack them face-to-face (F2F) using hybrid copper bonding *TechPowerUp, February 2026* |

| | |
|---|---|
| SAMSUNG | "Samsung, SK Hynix reportedly ramp hybrid bonding push for next-gen HBM" *Digitimes Asia. April 2026*<br>"Samsung unveils HBM4E, showcasing comprehensive AI solutions, NVIDIA partnership and Vision at NVIDIA GTC 2026" *Samsung. March 2026*<br>"Samsung Electronics launches silicon photonics foundry business." Building production ready photonic integrated circuits now with aim to scale toward co-packaged optics by 2030" *Design & Reuse. April 2026* |
| Micron | "How Micron is Looking to Win the HBM Wars" Micron frames hybrid bonding as part of its 2026 HBM4 transition. *Forbes. April 2026* |
| | "Apple M5 Pro and M5 Max Debut New M-Core Tier and SoIC 2.5D Packaging". The new SoIC-MH 2.5D technology from TSMC uses advanced copper-to-copper (Cu-Cu) bonding. *TechPowerUP. March 2026* |
| COHERENT | "Coherent demonstrates multiple co-packaged optics technologies at OFC 2026." Coherent to show how photonics stack can meet bandwidth and efficiency needs of AI datacenters. *Coherent. March 2026* |
| AMD | "Engineering the Future of AI" AMD has ongoing innovation in 2.5D, 3D and hybrid bonding as part of heterogeneous packaging for future Instinct accelerators. *AMD Blog. November 2025* |
| intel | "Intel Xeon 6+ Clearwater Forest is Out". Clearwater Forest uses compute tiles, base tiles, I/O tiles, EMIB, and Foveros Direct 3D packaging (hybrid bonding). *ServeTheHome. June 2026* |

# Hybrid Bonding Customer Adoption Expanding

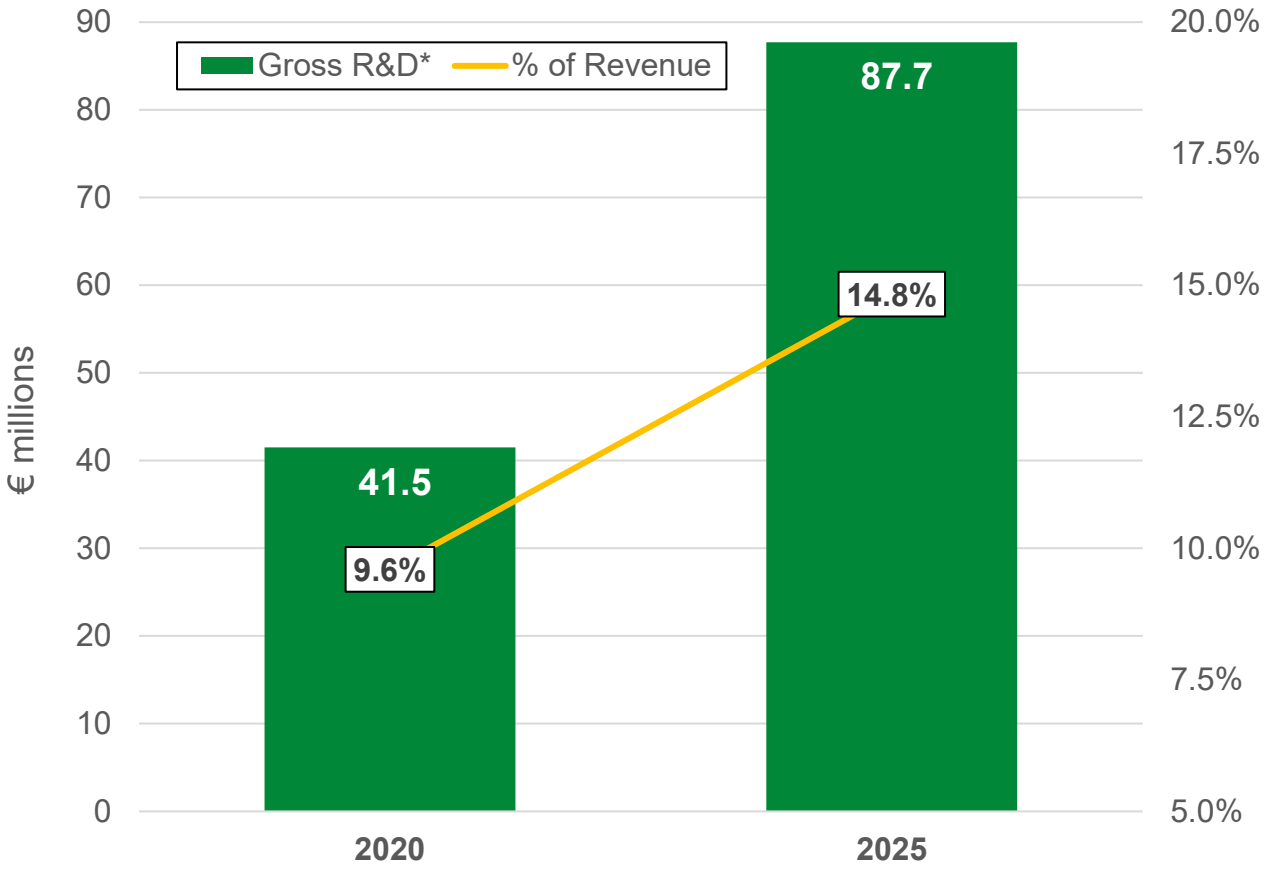



* Through Q1-26

- **Continued growth in HB adoption:**
  - 20 total customers
  - Customer mix skewed to logic currently via two leading customers
  - Other 18 customers represent important source of future demand
- **Cost of ownership differential versus TCB reducing**
  - Increased system maturity, increased yields and higher throughput
  - Thermal resistance performance up to 30% less than TCB as per recent customer benchmark

# Increased R&D Efforts Support Besi's Next Gen AI System Portfolio

## R&D investment has more than doubled since 2020




* Gross R&D spending excludes impact from capitalization/amortization of R&D costs

**Significant R&D investment in advanced packaging over past 5 years:**

- R&D spend expected to reduce as % of revenue during plan period

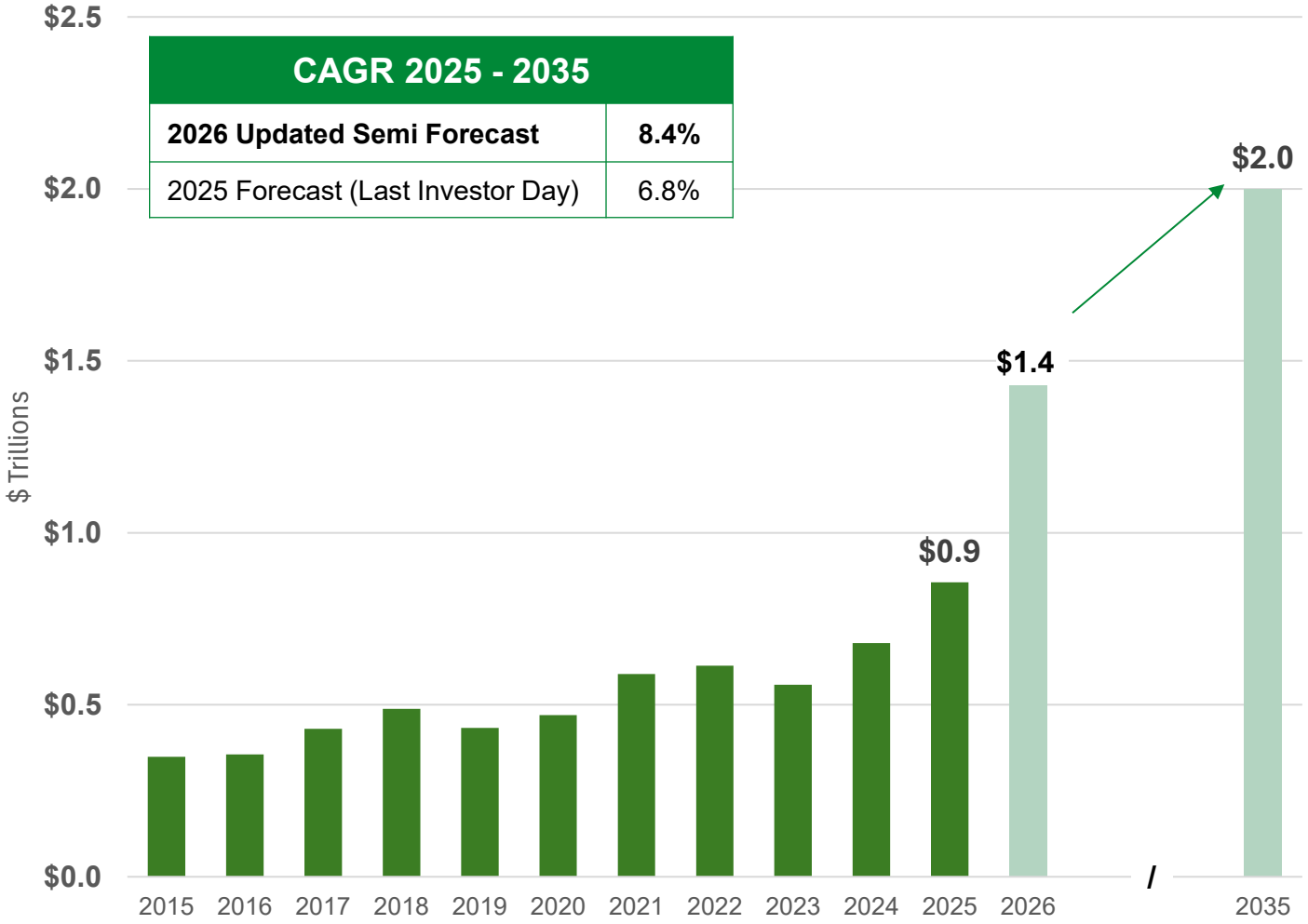
**Key areas of current focus:**

- **Hybrid bonding:**
  - 50 nm accuracy hybrid bonder in evaluation this year
  - Targets increased throughput (+50%) vs. Gen 1
- **Fluxless TCB with submicron accuracy:**
  - Expanded adoption beyond HBM including 2.5D CoWoS and certain CPO architectures
- **Flip chip/Multi module attach:**
  - Marketing next generation flip-chip bonder for 2.5D CoWoS
  - Extending flip-chip and TCB capabilities to CoPoS
  - Upgrading Evo platform to increase market share for photonic transceivers and CPO
    - 1 µm accuracy
    - 300 mm wafer processing

# II. MARKET TRENDS
## Chris Scanlan
## Senior VP Technology

# AI Driving New Semiconductor Super-cycle

## Annual Semiconductor Revenue Growth




| CAGR 2025 - 2035 | |
|---|---|
| **2026 Updated Semi Forecast** | **8.4%** |
| 2025 Forecast (Last Investor Day) | 6.8% |

Source: TechInsights, Q2-2026

### AI Infrastructure

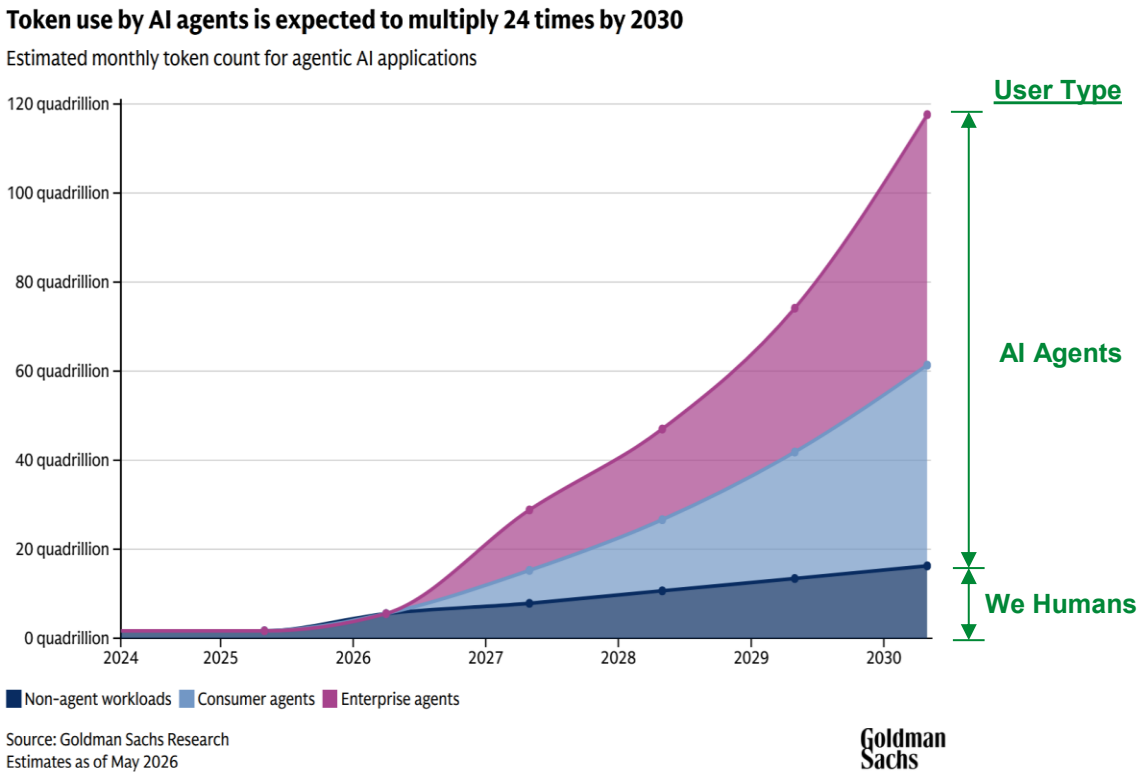
- LLM Training
- AI Inference

### AI Enabled Devices

- Mobile Devices
- Computers
- Robotics
- Self-Driving Cars

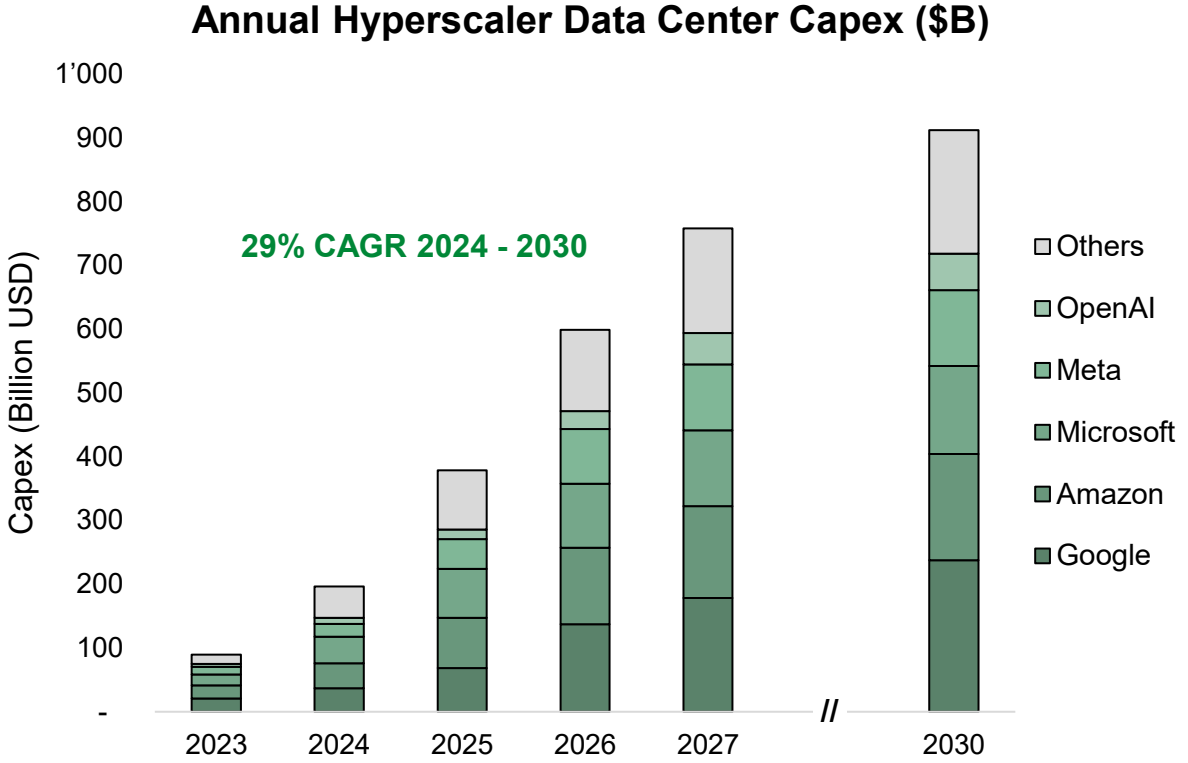
# Rapid AI Deployment and Market Adoption Require Large AI Infrastructure Investment by Hyperscalers

## AI model performance and usage growing exponentially




- Generative AI adopted faster than any previous technology
- Automated AI agents accelerate AI token usage
- Human duration of software development tasks that AI can do successfully is doubling every 7 months (METR.org 2026)

## Requiring big investment in computing infrastructure




Source: TechInsights Q2 2026

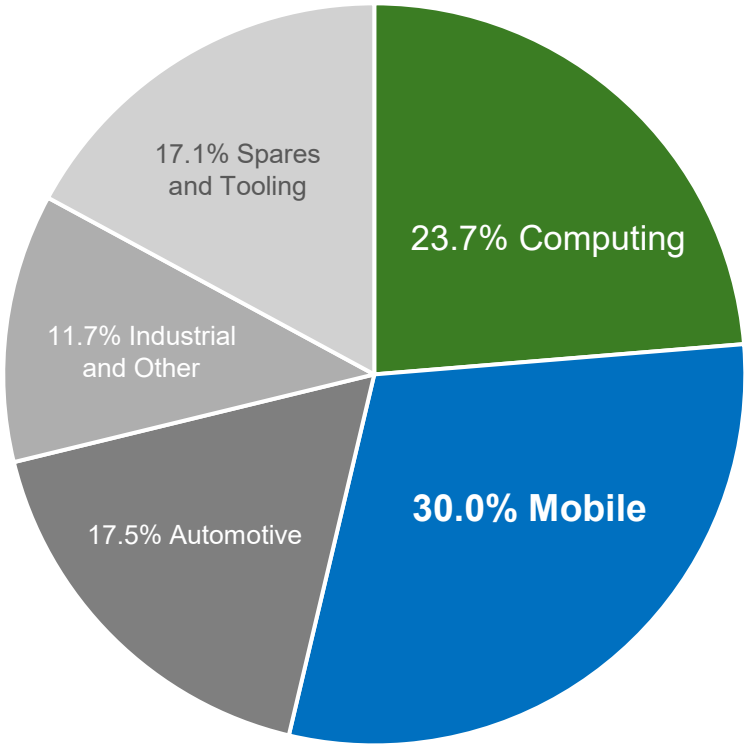
- AI infrastructure spending to exceed $1T by 2029 (IDC. April 2026)
- Global AI computing capacity is doubling every 7 months (EPOCH AI, Jan 2026)
- Data centers are projected to represent 3% of global energy consumption by 2030 (Gartner Nov 2025)

# Computing is Now Besi's Largest End-User Market

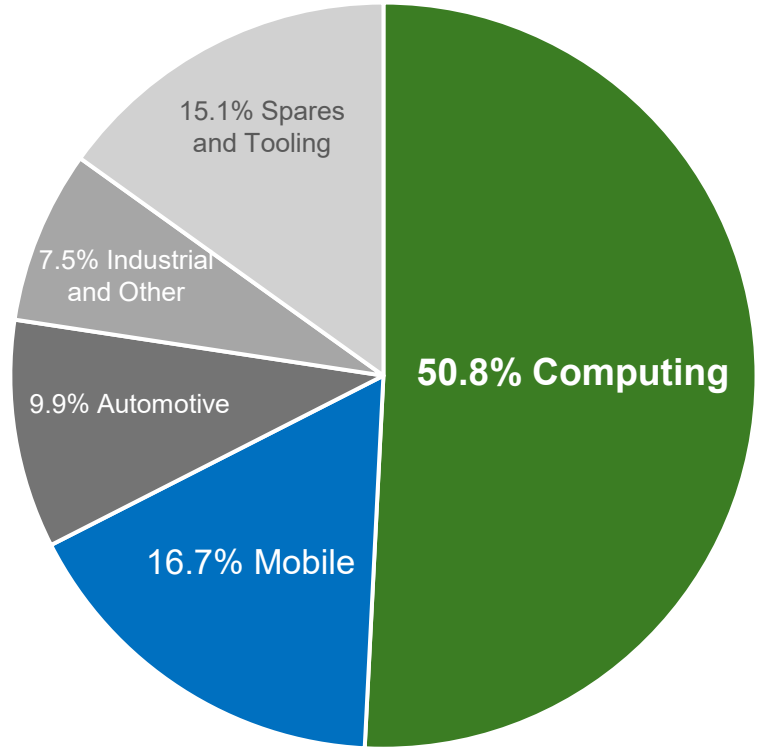
## Computing has grown to represent majority of Besi's end market revenue in 2025

Strong demand for advanced packaging capacity to support expansion of AI data centers and new AI enabled devices

### 2023 Besi End-User Market Composition




### 2025 Besi End-User Market Composition

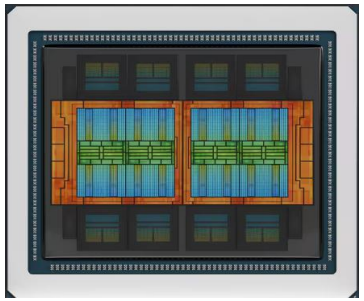
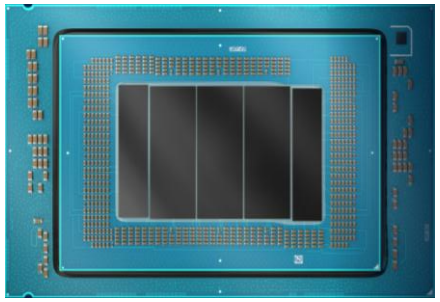
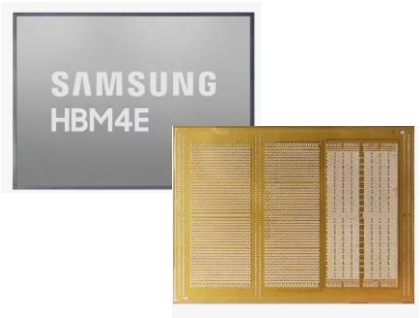
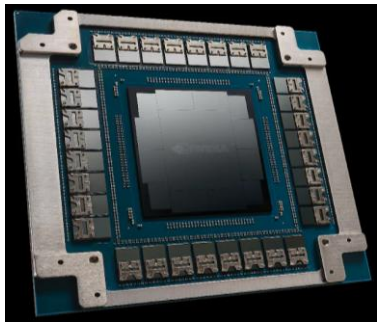


# AI Infrastructure Build-out Drives Demand for High Performance Computing Devices Using Advanced Packaging

New **AI Factories** link thousands of GPU servers together to make **entire data centers function as one computer**

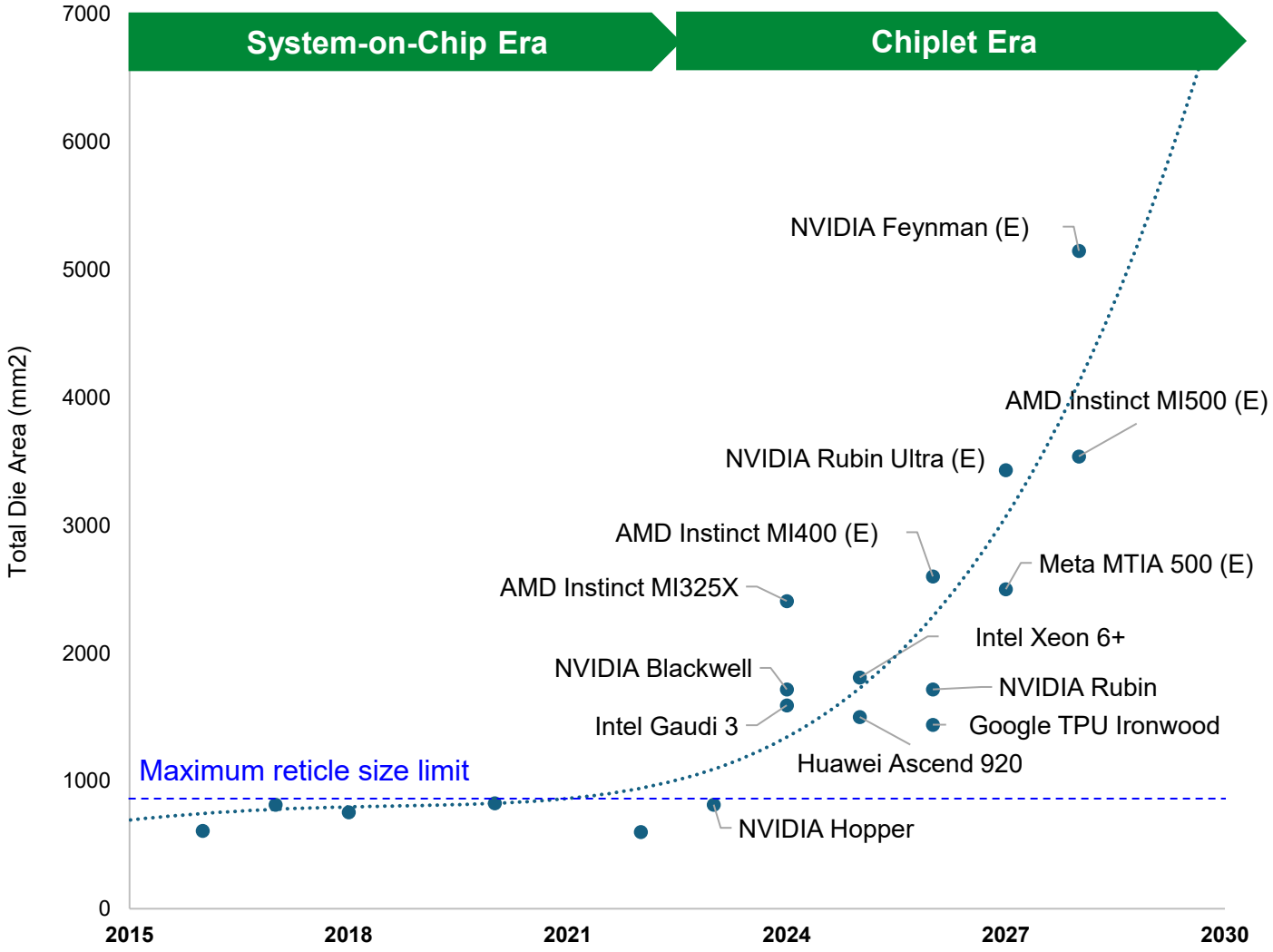
Source: NVIDIA

Which drives significant demand for high performance processors, memory and networking devices **using advanced 2.5D & 3D packaging**

| GPUs & Accelerators | CPUs | HBM Memory | CPO Network Switches | Photonic Transcievers |
|---|---|---|---|---|
|  Source: AMD AMD MI355x Accelerator |  Source: Intel Intel Xeon 6+ CPU |   Source: Samsung HBM4E |  Source: NVIDIA NVIDIA Spectrum X Switch |  Source: NVIDIA Ethernet Transceiver |

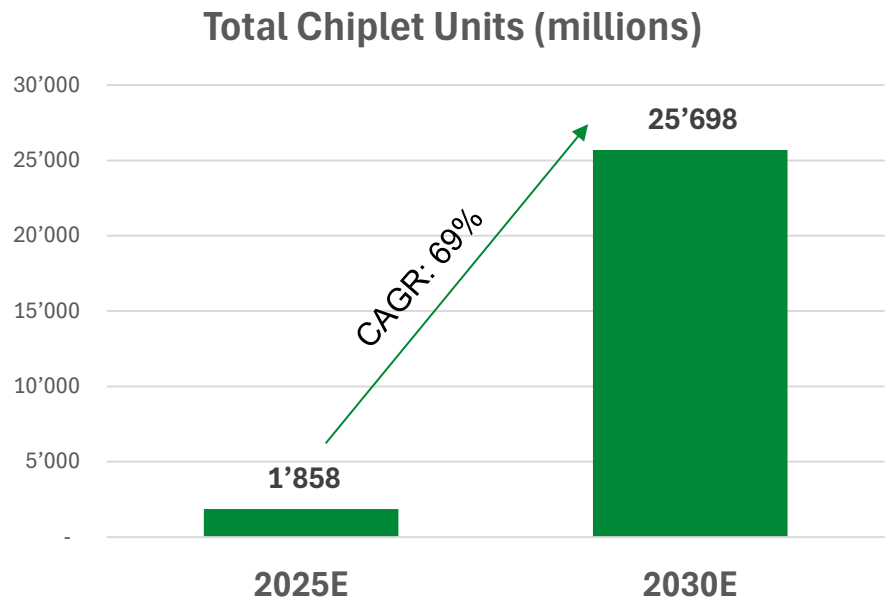
# Chiplet Adoption Accelerating as Size of Silicon Area Increases

## Latest AI Devices Require Multiple Chiplets with 2.5D/3D Packaging




Source: AMD, NVIDIA, Intel, TrendForce, Besi Estimates

- **High performance devices adopting chiplets** as die sizes exceed maximum reticle size for single SoC chips
- **Chiplet adoption growing rapidly**, increasing number of die attach steps required and demand for advanced die attach equipment




Source: TechInsights 2026

# Hyperscalers Are Also Developing Their Own Custom AI Devices

**Custom accelerators and CPUs being optimized for specific use cases and to lower cost per token**

Large devices integrate multiple chiplets in 2.5D and 3D advanced packaging chiplets

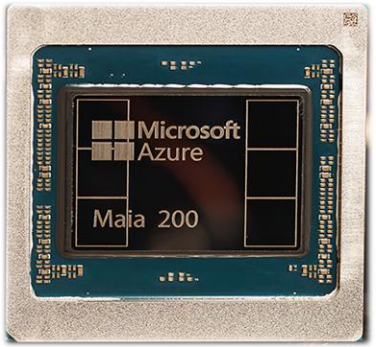
## Google TPU 8t


**Accelerator for AI training**

## Amazon AWS Tranium


**CoWoS-R**

## Microsoft Maia 200




**CoWoS-S**

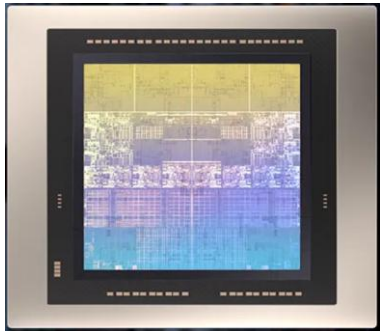
## Google TPU 8i


**Accelerator for AI inference**

## Meta MTIA 500 Accelerator

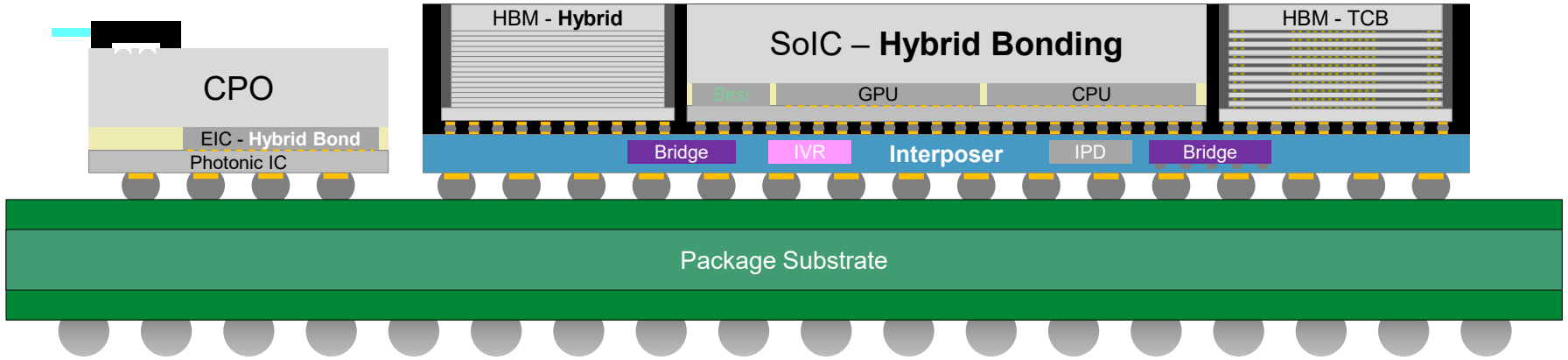
**CoWoS-S**

## Alibaba Cloud Zehnwu M890



**2.5D (CoWoS-like)**

# Besi Offers Complete Portfolio for Complex AI Chiplet Packages

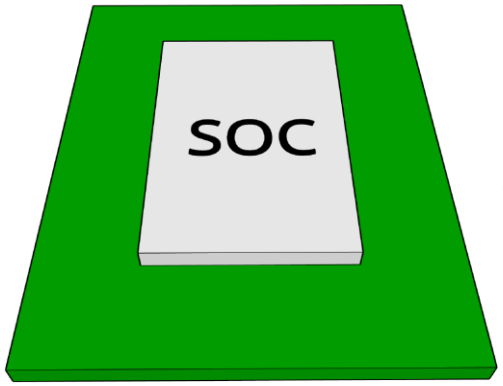



| Hybrid Bonding | CoW Flip-chip & Bridge | Fluxless TCB | CoS Flip-chip | oS and Photonics |
|---|---|---|---|---|
|  |  |  |  |  |
| **8800 CHAMEO** UltraPlus AC | **8800 CHAMEO** fLex | **9800 TC Next** | **8800 Quantum** AdvX | **2200 evo** |

# Increasing Packaging Complexity Also Driving Higher Capital Intensity

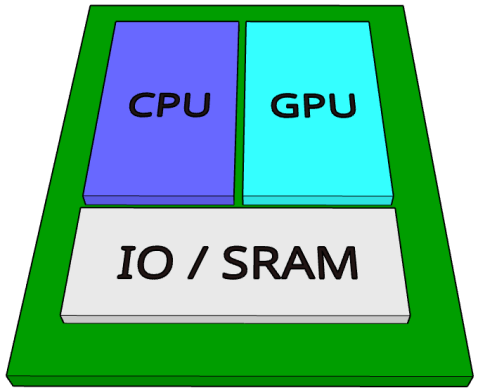
Besi

**Single Chip Design**



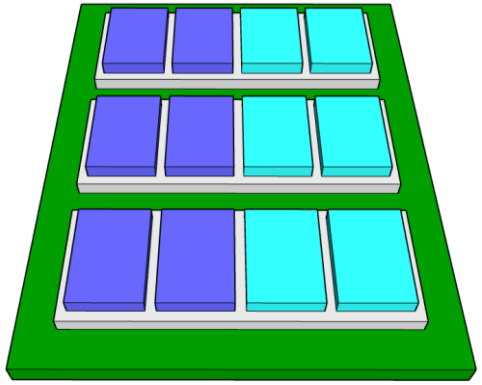

**Monolithic:** Integrated SoC

**Multi-Chip Module**



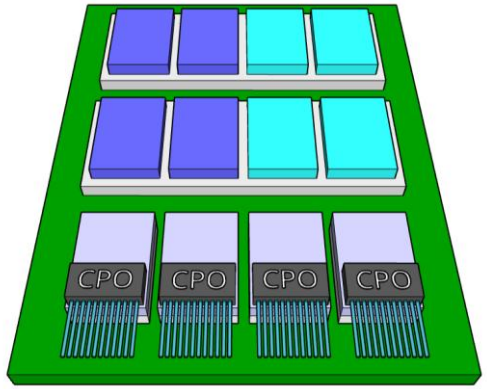

**Multiple Dies**

**3D Chiplet System**



**2.5D / 3D Interconnect**

**Co-Packaged Optics**



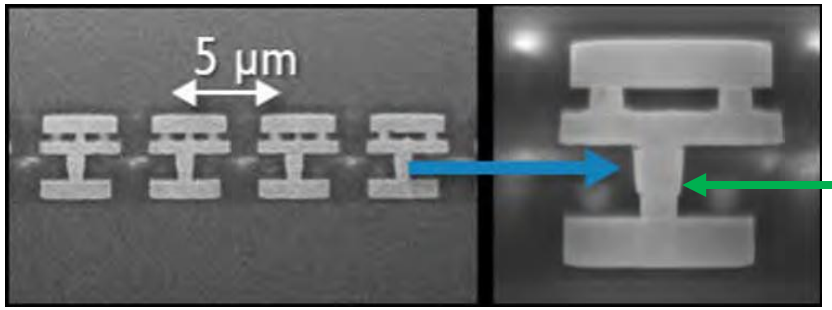

**Add Optical Interconnects**

**Requires increased number of die attach steps and higher accuracy**

# Hybrid Bonding is Technology of Choice for High Performance 3D Heterogeneous Integration

## Hybrid Bonding is extension of front-end fab process

Directly connects chips in 3D with highest interconnect density

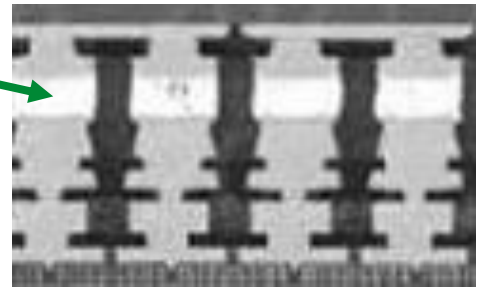



Direct, gapless Cu to Cu bond

Source: AMD

## TCB uses µ-bump interconnect to connect chips with solder and epoxy encapsulation materials

Solder µbumps with gap fill material



- **Lower bump density**
- **Higher thermal resistance**
- **Back-end assembly process**

Source: Intel

## Hybrid Bonding Benefits for 3D Chip Stacking

- ✓ 15X Higher Interconnect Density[1]
- ✓ 11.9X Higher Speed[1]
- ✓ 191X Higher Bandwidth Density[1]
- ✓ >100X Higher Energy Efficient Performance[2]
- ✓ Up to 30% Lower Thermal Resistance[3]
- ✓ Higher Reliability Performance[4]
- ✓ 10X Lower Cost per Interconnect[4]

Notes: 1) TSMC, 2023 ECTC, 2) TSMC 2025 ECTC, 3) Samsung 2026 ECTC, 4) Besi Company Analysis

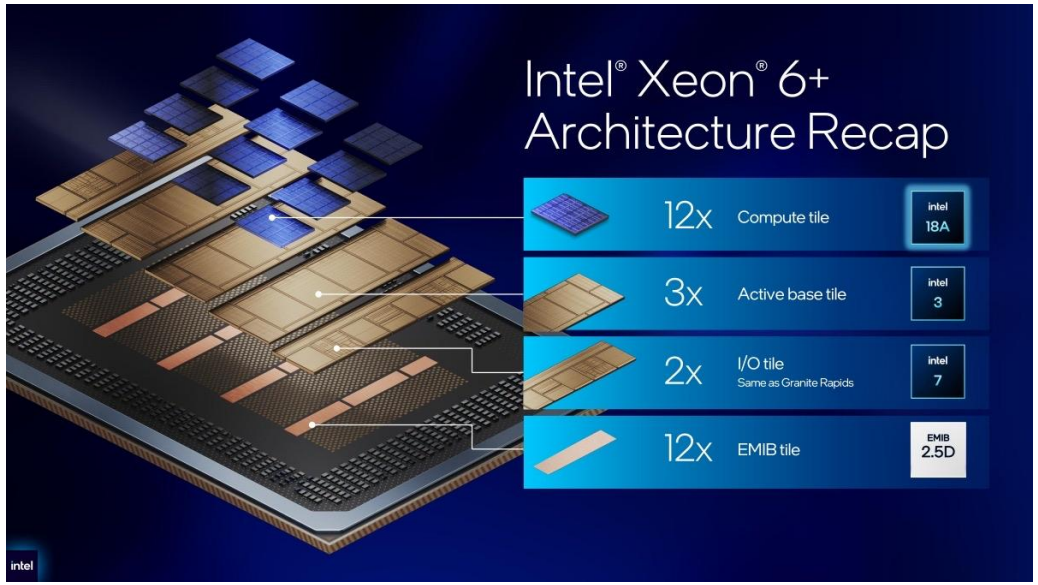
# Hybrid Bonding Solves SRAM Bottleneck in Data Center XPUs

## More SRAM capacity is needed to improve performance of both CPUs and AI Accelerators

Not cost effective to use more advanced nodes for SRAM as performance does not scale below 5nm node

**Hybrid bonding solves problem** by stacking advanced node core chiplets onto lower cost, trailing node SRAM chiplets

### Intel Xeon 6+ Data Center CPU




Source: Intel

**CPU Core Function Design in Most Advanced 18A Node**

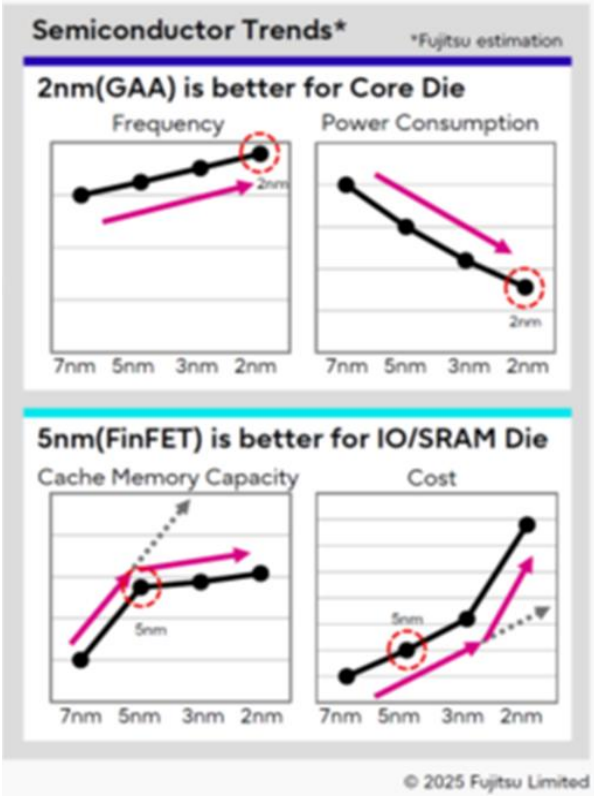
- Hybrid bonded onto base tiles with SRAM and other functions
- Limits expensive advanced node usage only to critical core compute

### Fujitsu (Broadcom) Monaka CPU Using Hybrid Bonding


Source: Fujitsu

**Hybrid Bonding Reduces Total Wafer Cost**

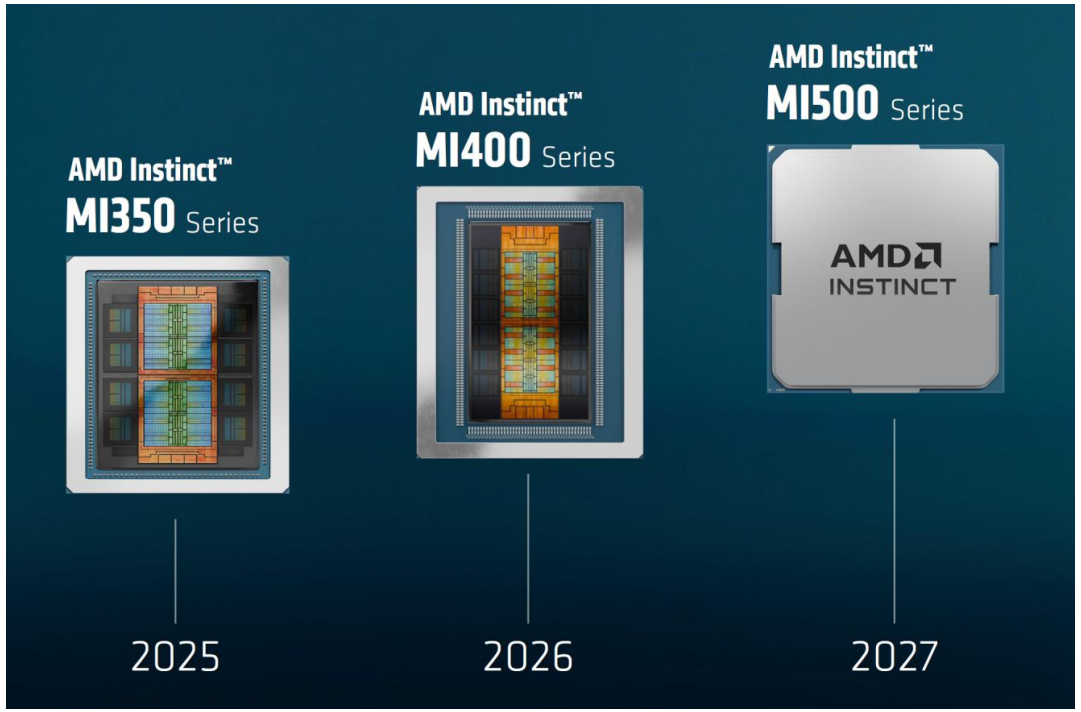
- Only 30% of die area used in 2nm node
- SRAM and IO die use 5nm node



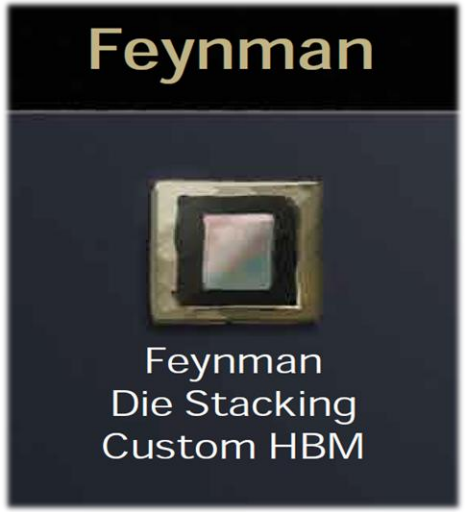
# Increased Use of Hybrid Bonding in GPUs and Accelerators Expected

## AMD expanding use of hybrid bonding in AI accelerators

- MI355X with 6 µm pitch hybrid bonding now in HVM
- Stacking of accelerator chiplets to I/O and SRAM die



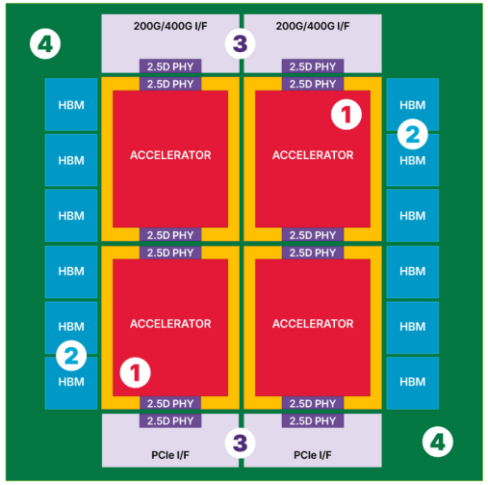

Source: AMD




Source: NVIDIA

## NVIDIA's next generation Feynman (2028) has multiple potential hybrid bonding use cases

- Feynman GPU with 3D die stacking
- Introduction of customized HBM



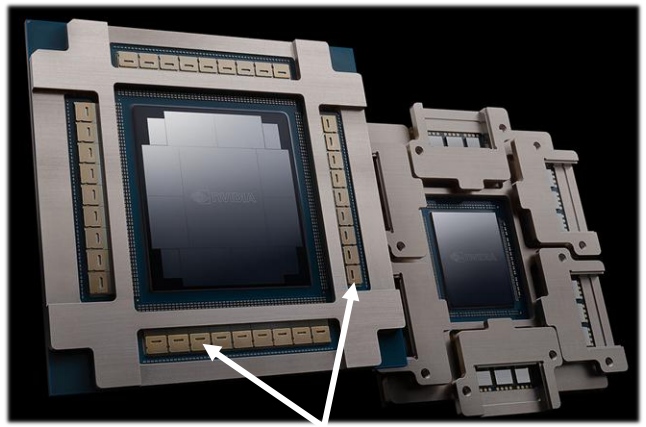

Source: Broadcom

## Broadcom's 3.5D XDSiP

- Hybrid bonding of accelerator chiplets to I/O and SRAM die
- In development for multiple hyperscaler customers

# Hybrid Bonding Becoming Standard for CPO Chiplets in AI Factories

## Co-Packaged-Optics based on TSMC's COUPE with hybrid bonding now in HVM in leading scale-out network switches



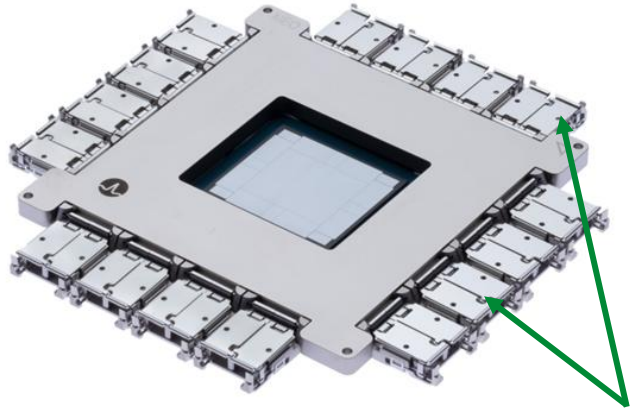
**NVIDIA's CPO switches using COUPE**

Source: NVIDIA

CPO performance significantly higher compared to traditional pluggable transceivers*:

- ✓ **3.5x power efficiency**
- ✓ **10x higher resiliency**
- ✓ **1.3x faster installation time**

*NVIDIA, 2026 Hotchips



**Marvell's Tomahawk 6 CPO switch using COUPE**

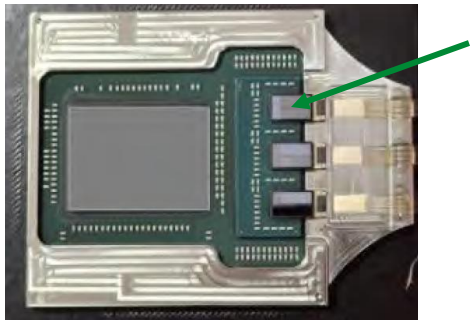
Source: Marvell

## Increased hybrid bonding potential in scale-up networking. CPO will directly connect GPUs to each other within the rack


Source: NVIDIA

**NVIDIA's Feynman** platform adds CPO to connect GPUs

**NVLink 8 CPO** is scale-up switch connecting multiple GPUs, replaces copper wiring



Source: AMD

CPO chiplets integrated in GPU package

- ✓ Higher bandwidth
- ✓ Lower power
- ✓ Lower latency

# Hybrid Bonding Adoption Expected in HBM4e, HBM5 and Custom HBM

**"HCB technology not only enables a higher number of I/O and performance improvements but also significantly enhances thermal behavior"** – *Samsung, 2026 IEEE ECTC*

**"Hybrid Copper Bonding thus emerges as a required path for next-generation GPUs approaching and exceeding 2 kW+"**
*Samsung, 2026 IEEE ECTC*

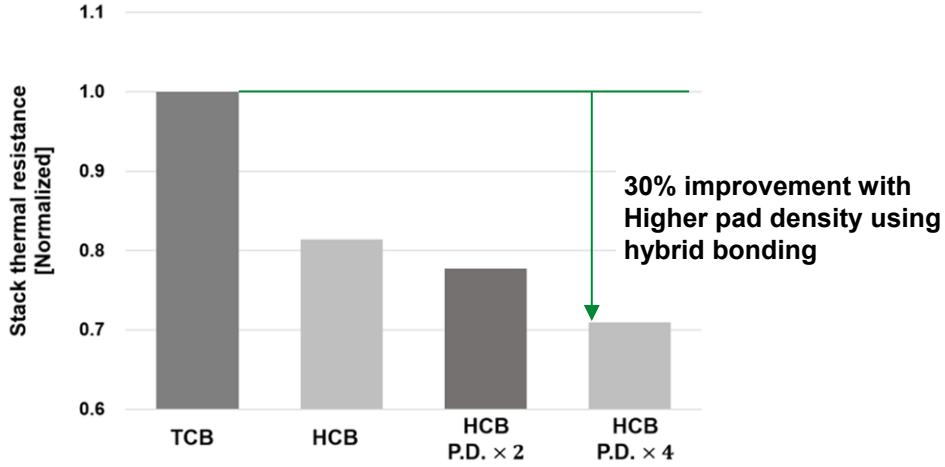
**Hybrid bonding on track for 1st production in HBM4e in 2027**

- Expected to be used in majority of HBM5 and custom HBMs

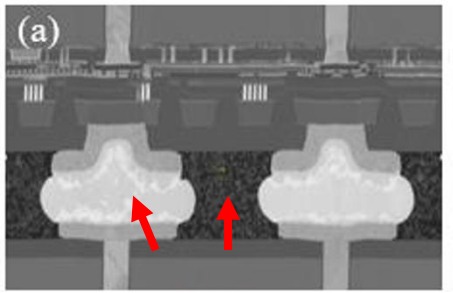
**Benefits of hybrid bonding for HBM memory stacking:**

- ✓ Better thermal performance
- ✓ Higher interconnect density for custom HBM
- ✓ Improved energy efficiency, latency and speed
- ✓ Scalable to higher stack densities

**Thermal resistance of HBM with Hybrid Bonding up to 30% better than TCB**

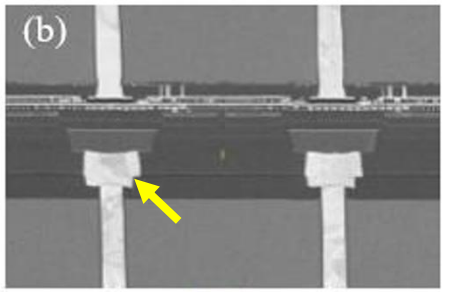



**TCB µbump**




**High resistive materials used in gaps between chips**

**Hybrid bonding**




**Gapless connection with low resistance**

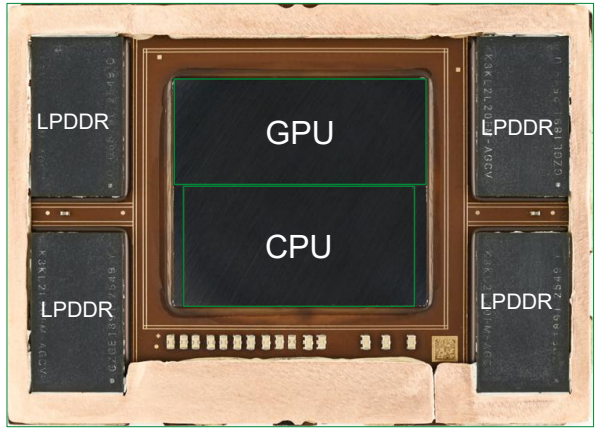
*Samsung, 2026 IEEE ECTC*

# Hybrid Bonding Expanding Into High-End Consumer Computing

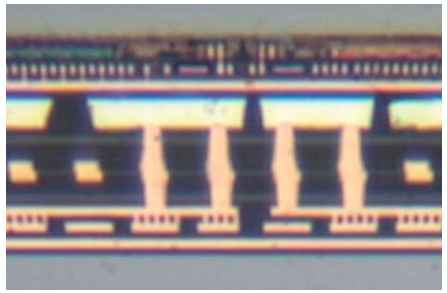
## High-end consumer PC chips using hybrid-bonded chiplet architectures in HVM

### Fusion Architecture introduced in 2026 M5 Pro and M5 Max laptops

- Hybrid bonding of separate CPU and GPU chips to Si base die to form a single SoIC with very low die-to-die latency



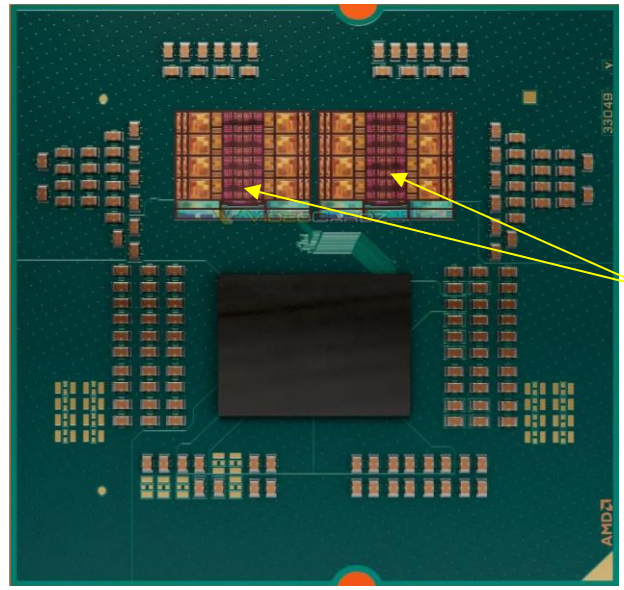

Source: TechSearch International




Source: TechSearch International

- Hybrid bonding combines a common CPU chiplet with different GPU chiplets (e.g. Pro and Max)
- Reduces die cost and increases yield by dividing chip design into 2 smaller chips

### AMD Ryzen™ 9 9950X3D2 Latest Version PC Gaming CPU




Source: AMD

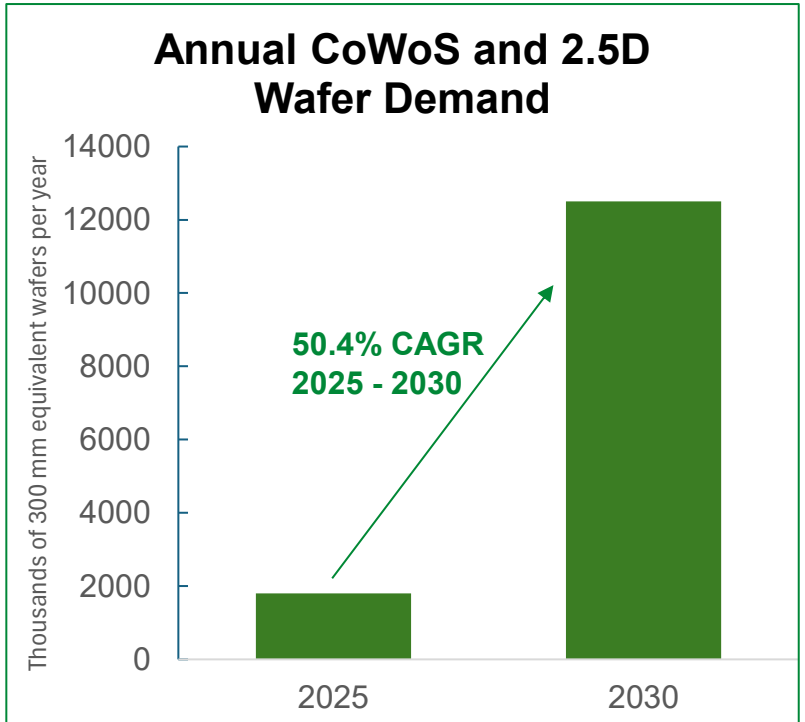
- First gaming CPU with 2 hybrid bonded CCD chiplets

# 2.5D (CoWoS) Demand is Also Expanding Rapidly, Exceeding Supply

## CoWoS & 2.5D capacity growing rapidly, driven by demand for AI chipsets

Capacity expansion in progress by both foundries and OSATs:

- Requires wafer-level assembly (CoW) of chiplets and bridge chips using flip-chip or TCB processes
- And placement of assembled interposer modules onto package substrate (oS)




Source: TechSearch 2026

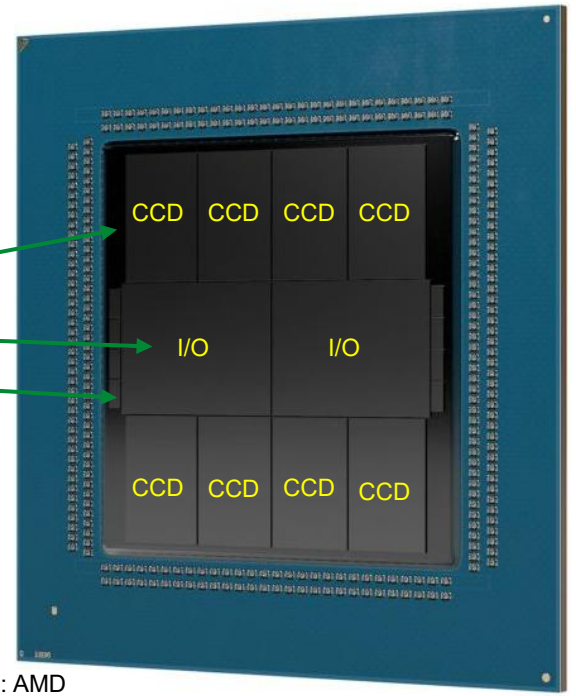
**AMD Next Generation Venice CPU**

Q4 2026

CoWoS package combining:

- 8 compute chiplets on N2P node
- 2 I/O chiplets on N6 node
- 8 Integrated passive chips

CCDs with hybrid bonded 3D V-cache
Expected in Venice-X (2027)




Source: AMD

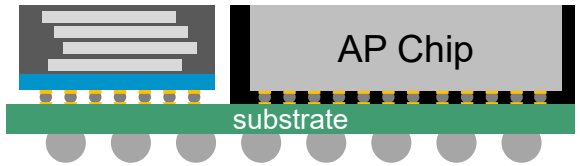
# Edge AI Applications Present Additional Growth Opportunities

**New consumer devices, such as AI-enabled mobile phones, smart glasses, and other wearables drive opportunities for Besi's advanced packaging portfolio**

## Mobile Application Processors

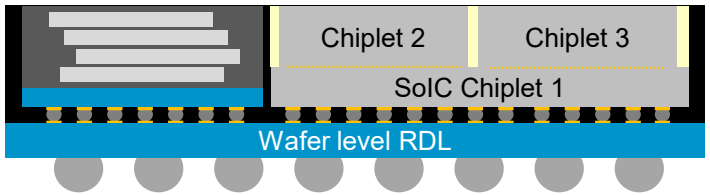
New AP packages for AI smart phones with **advanced flip-chip & molding**

Side-by-side AP & memory (2026-27)




Next gen wafer level assemblies with multiple chiplets (WMCM)

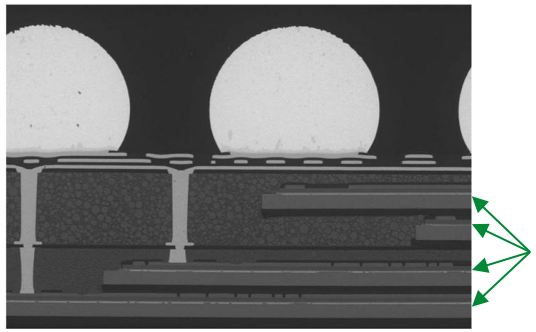
Wafer-level MCM, eliminates substrate




## Mobile Memory

New wafer level 3D packages in development for mobile LPDDR

Requires high accuracy, high speed **chip-to-wafer die stacking**



4 LPDDR die w/ high accuracy C2W die attach*

Compared to current technology*

- ✓ **2x higher I/O density**
- ✓ **2.7x higher bandwidth**
- ✓ **25% thinner package**

*Source: Samsung 2025 ECTC

## Smart Eyewear

Smart eyewear market growing at 24% CAGR 2026 – 2033

Source: Warby Parker

Miniaturized 2.5D and 3D packaging

Source: Meta

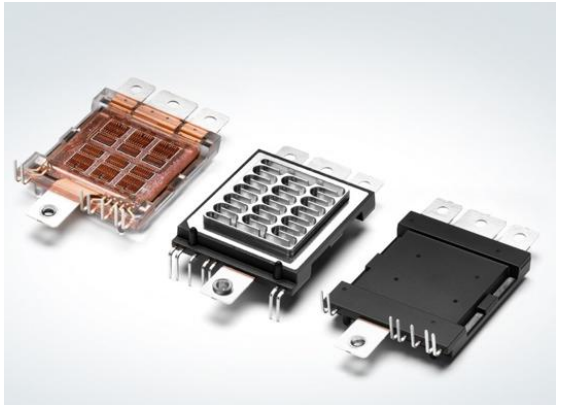
Future **hybrid bonding** for displays

# AI Also Driving Growth in Mainstream End Markets

## Automotive

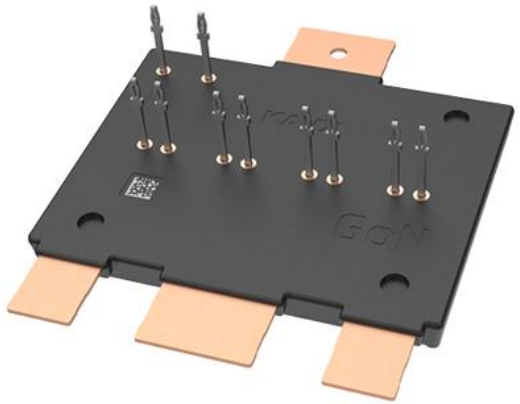
- **Automotive semiconductor market projected to grow at 8% CAGR 2025 to 2030** (TechInsights 2026)
- Driven by growth in EV vehicles and automomous driving with higher semiconductor content per vehicle

SiC (Silicon Carbide)



Source: Semicron Danfoss

GaN (Galium Nitride)



Source: Kyocera AVX

SiC and GaN traction inverters for EV power train require **MMA die attach and high precision molding and packaging**

## Data Center Power Management

AI servers drive significant demand for high-efficiency power management ICs


Source: Vicor


Source: Infineon


Source: MPS

**Diffusion die bonding and high precision molding**

## Microcontrollers for Physical AI

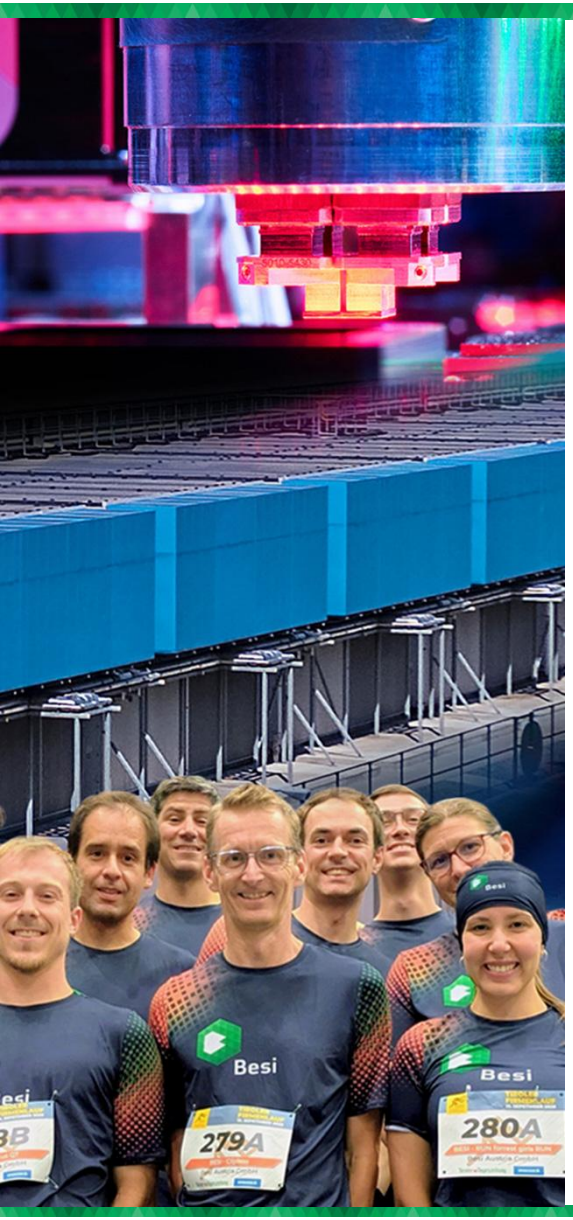
New class of NPU-accelerated MCUs enables AI functionality for robotics and other physical AI devices

Source: Intel


Source: ST Micro

# Market Trends Summary

| | |
|---|---|
| ✓ | **Besi's leading edge product portfolio well positioned** to gain market share |
| ✓ | Rapid advancements in AI technology and adoption **driving growth in all of Besi's end-user markets, particularly computing** |
| ✓ | **Chiplet architecture adoption accelerating** as Moore's Law slows |
| ✓ | **Hybrid bonding is highest-performance, most energy-efficient interconnect technology** for next-gen devices with lowest cost per interconnect |
| ✓ | **Hybrid Bonding applications, use cases and customer adoption expanding** |
| ✓ | **Capacity expansion in 2.5D packaging** creates significant market potential for Besi's C2W flip-chip, Advanced TCB, MMA |
| ✓ | **Photonics becoming high growth application** for hybrid bonding and MMA assembly processes |
| ✓ | **Edge AI presents additional growth opportunities** in automotive, data center, and power management |




# III. WAFER LEVEL ASSEMBLY

## Peter Wiedner

## Senior VP Sub-Micron Die Attach

# ECTC 2026: Hybrid Bonding Is Pulling Packaging Into Front-End

Besi

"**Memory bandwidth, chiplet-to-chiplet latency, synchronization overhead and energy per bit** now shape overall efficiency in multi-die (AI) architectures.

In that environment, **how efficiently dies exchange data** increasingly determines how far a system can scale.

***Hybrid bonding directly attacks all those bottlenecks.***"

Huan Ma from "Advanced Packaging Debrief" ECTC June 8, 2026

# Besi Hybrid Bonder - Roadmap for Sustained Leadership

**1** **8800 CHAMEO ultra plus**
**First HVM Hybrid Machine**
**Accuracy: 200nm**

**Logic** Bump Pitch: 9µm

**2** **8800 CHAMEO ultra plus AC**
**Today's Industry Standard**
**Accuracy: 100nm**

Bump Pitch: 6µm

**Memory** UPH: 1,500

**3** **3300 HYBRID N50**
**Beta test starting 2026**
**Accuracy: 50nm**

Bump Pitch: 3µm

UPH: 3,000

**4** **3300 HYBRID**
**In Development**
**Accuracy: 25nm**

Bump Pitch: <1µm

UPH: ++++

APPLIED MATERIALS

Besi

- Integrated KINEX system improves yield in stacked and complex applications
- Adoption of integrated lines enhances Besi's competitive position

# Applied Materials & Besi Collaboration Helps Accelerate Hybrid Bonding Adoption and Growth

## CoE – Center of Excellence

- Dedicated AMAT-BESI Packaging Development Center in Singapore
- Equipped with two integrated lines and five hybrid bonders
- Collaborating to develop next generation hybrid processes
- Engaging with end customers to develop custom hybrid bonded devices

Collaborative Accelerated Innovation

**More than 25 customer engagements in Besi – AMAT COE**

# Hybrid Bonding Use Cases Confirmed for Logic Applications Adoption Expanding in Data Center and Consumer End Markets

Besi

tsmc intel SAMSUNG AMD BROADCOM NVIDIA Meta GLOBAL FOUNDRIES amazon Google Microsoft

**Roadmap:**

**Next generation logic devices will require bond pad pitches below 1µm**

- N50: next generation 50nm Bonder
- Starting Beta Test in Q4/2026


**Hybrid bonding becoming confirmed as predominant interconnect technology for AI Use Cases**

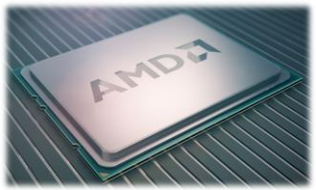
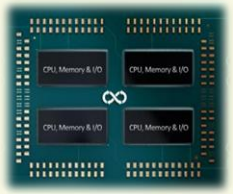
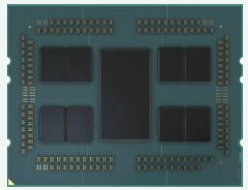
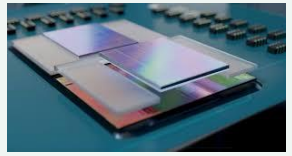
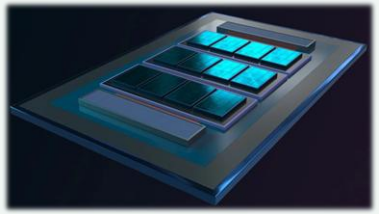
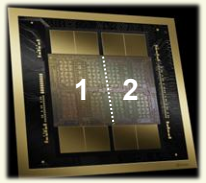
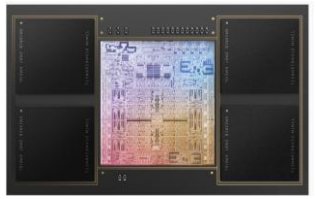
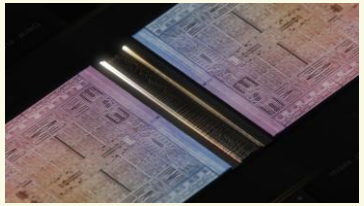
- **AMD** enlarging its device portfolio
- **Intel** recently launched first hybrid bonded product
- **Nvidia** announced Feynman family using hybrid interconnect
- Hyperscalers like **Meta** and **Google** designing proprietary AI XPUs
- New fabs being constructed in response to increased demand

**Hybrid bonding finding its way into high end personal computing applications**

- **Apple M5** chip now being manufactured with hybrid interconnect technology

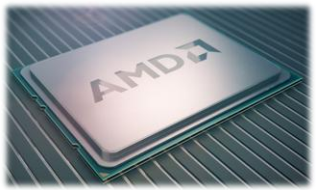
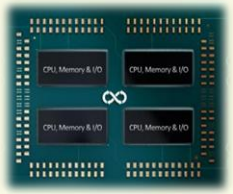
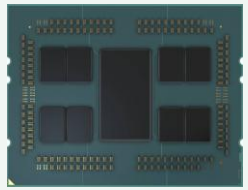
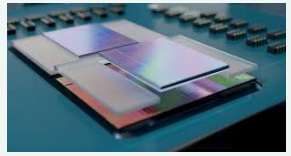
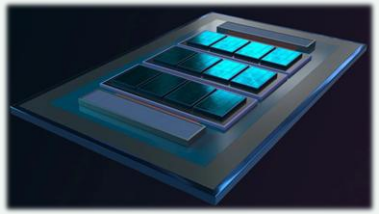
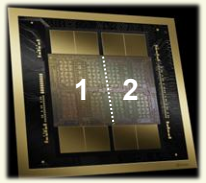
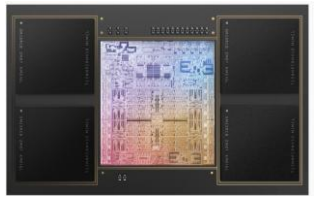
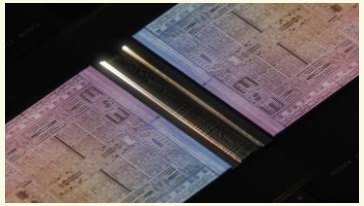
# 2024 Investor Day High Performance Processor Roadmap

Besi

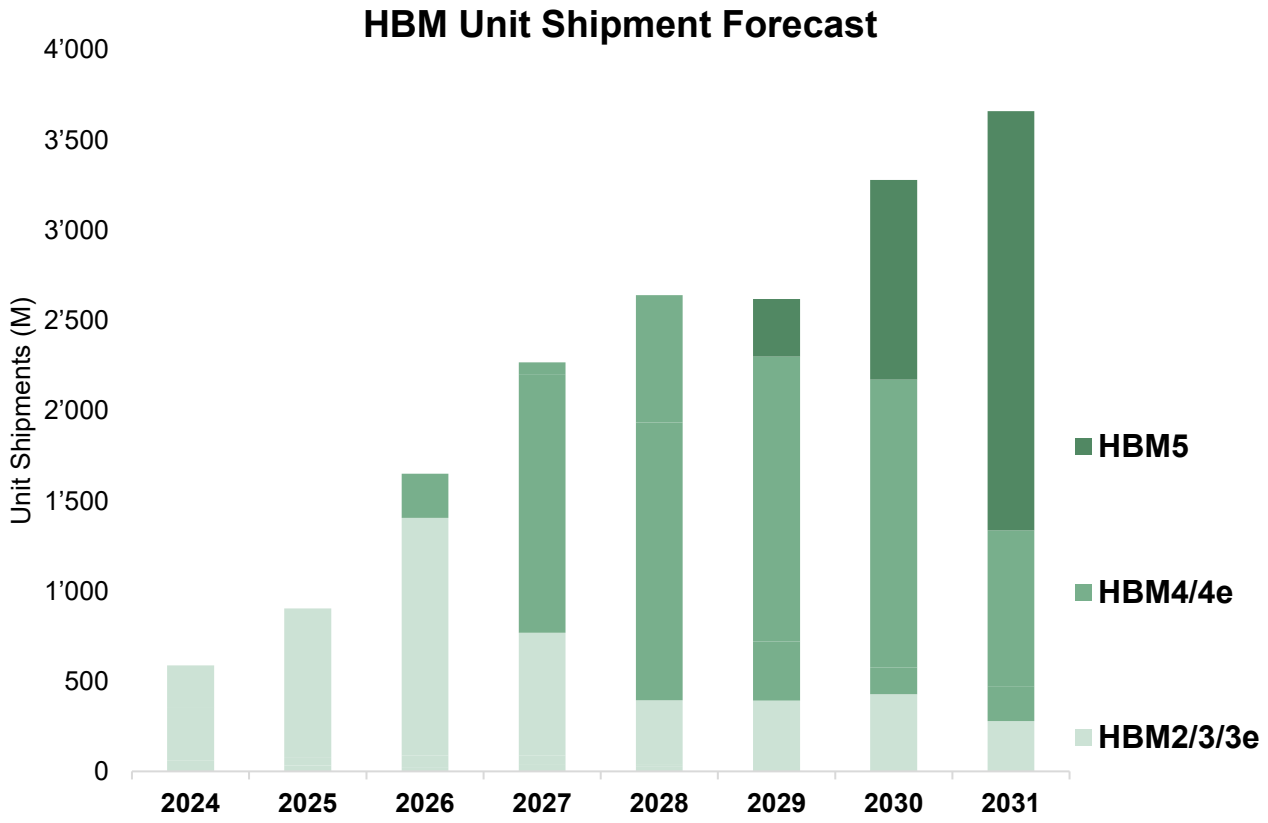
| | SoC | Split Die | Chiplets and Hybrid Bonding | |
|---|---|---|---|---|
| AMD | Opteron Server CPUs  | 1st Gen EPYC CPU (2017)  | 2nd Gen EPYC (2019)  | 3rd Gen EPYC (2022) with Hybrid Bonding  |
| intel | 3rd Gen Xeon CPU  | Sapphire Rapids CPU (2023)  | Clearwater Forest CPU w/ Hybrid Bonding  | |
| NVIDIA | H100 GPU  | B100 GPU (2024)  | Future chiplet architectures | |
| Apple | M1 Max CPU  | M1 Ultra CPU (2022)  | | |

# 2026 Update: Significant New Products Announced Over Past Year

Besi

| | SoC | Split Die | Chiplets and Hybrid Bonding | |
|---|---|---|---|---|
| AMD | Opteron Server CPUs  | 1st Gen EPYC CPU (2017)  | 2nd Gen EPYC (2019)  | 3rd Gen EPYC (2022) with Hybrid Bonding  |
| intel | 3rd Gen Xeon CPU  | Sapphire Rapids CPU (2023)  | Clearwater Forest CPU w/ Hybrid Bonding  | Xeon 6+ Launched |
| NVIDIA | H100 GPU  | B100 GPU (2024)  |   | Feynman Announced |
| Apple | M1 Max CPU  | M1 Ultra CPU (2022)  |   | M5 PRO M5 MAX Launched |

# First Insertion Point for Hybrid Bonding in HBM4e
# Customers Now Preparing For Volume Manufacturing in 2027




Source: TechInsights Q2 2026

SAMSUNG SK hynix Micron

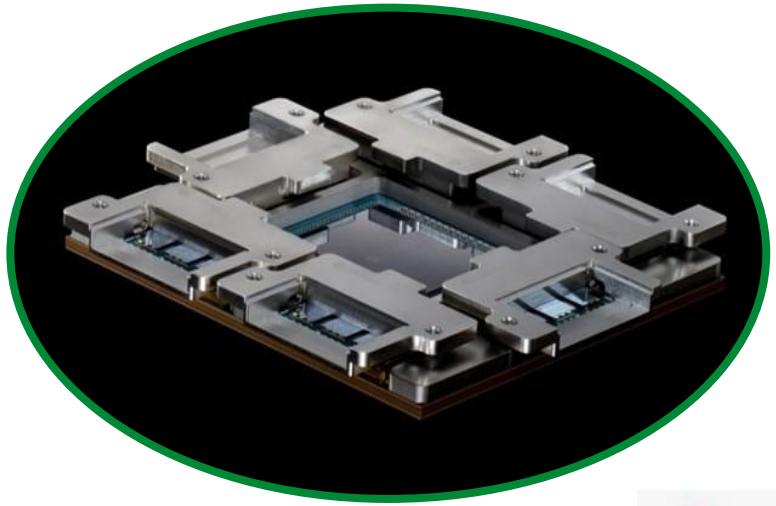
## Clear technical drivers for memory adoption:

- In parallel with HBM market growth, **key memory players developing lower power, faster and bigger memory packages**
- **Hybrid enables lower power consumption and better heat dissipation** (up to 30%), enabling higher memory stacks (>16 layers) and faster data exchange
- HBM with **custom logic base die** is **driving bond pad pitch down to 12 µm**

## Status Update:

- **All leading HBM players evaluating** Besi's hybrid bonding solutions
- **HBM4e is insertion point** for Hybrid Bonding in HBM stacking
- **First mover is preparing for HVM in 2027**
- **Hybrid and TCB will coexist**
  - Hybrid will take larger share in each successive generation

# Co-Packaged Optics is an Additional Hybrid Bonding Growth Driver



NVIDIA

BROADCOM

AyarLabs

tsmc

celestial AI now part of MARVELL

alchip

SAMSUNG

GlobalFoundries

fabrinet

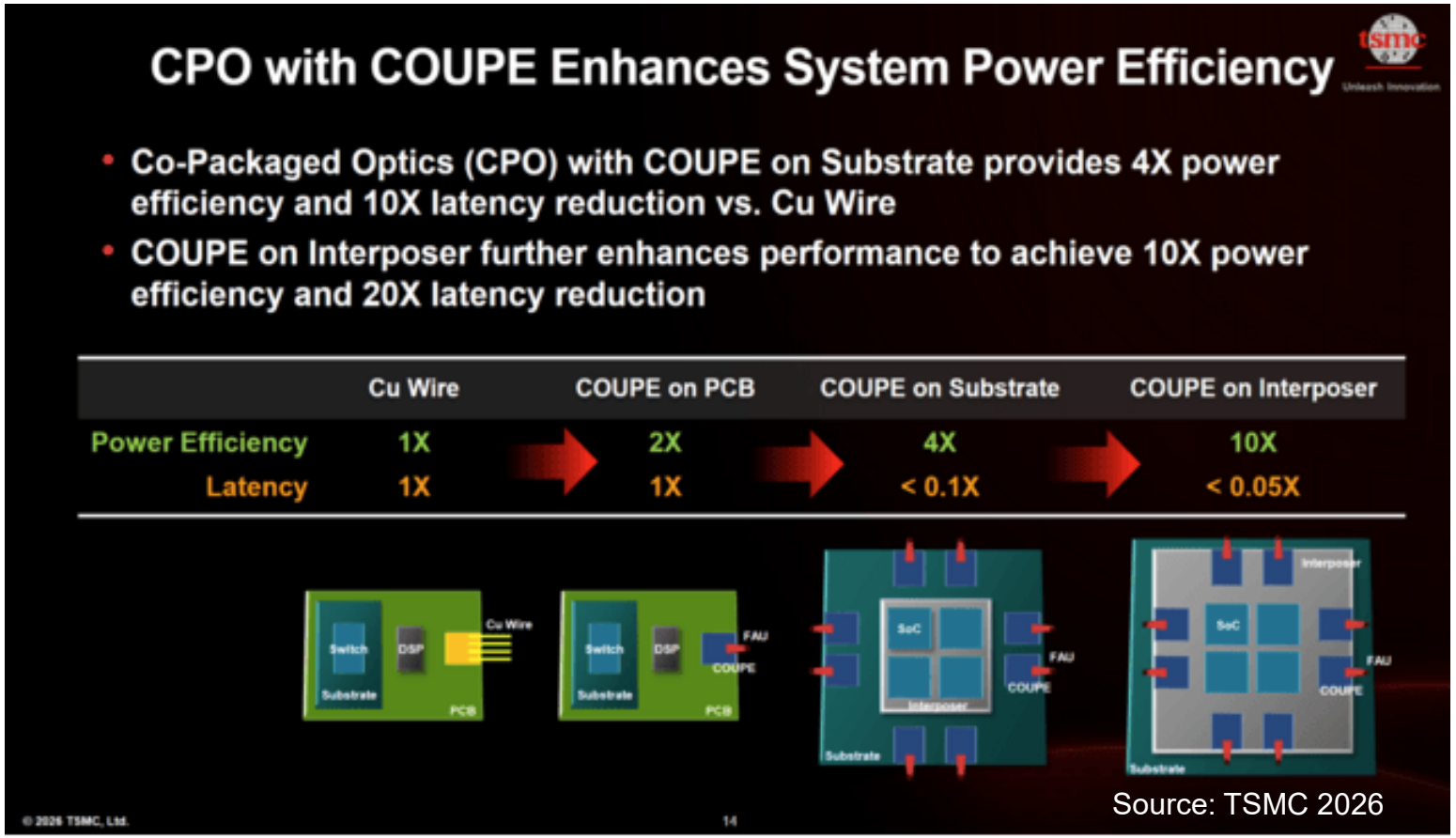
**Accelerating CPO demand drives additional hybrid bonding adoption:**

- **Hyperscalers looking for faster, lower power** data center connectivity
- Suppliers responding with **novel CPO package types** including hybrid interconnects (e.g. COUPE)

**Status Update**

- **First use cases announced** last year. **High volume manufacturing beginning:**
  - **Nvidia**: Spectrum-X and Quantum-X photonic switches
  - **Broadcom:** open Bailly CPO platform (eg: Tomahawk)
  - Traditional optical component suppliers such as **Coherent** and **Marvell** adapting their portfolios for CPO applications
  - **Ayar Labs** and **Celestial AI** pioneering novel hybrid bonded architectures

# TSMC's COUPE with Hybrid Bonding is Leading CPO Technology Offers Superior Performance, Energy Efficiency and Scalability

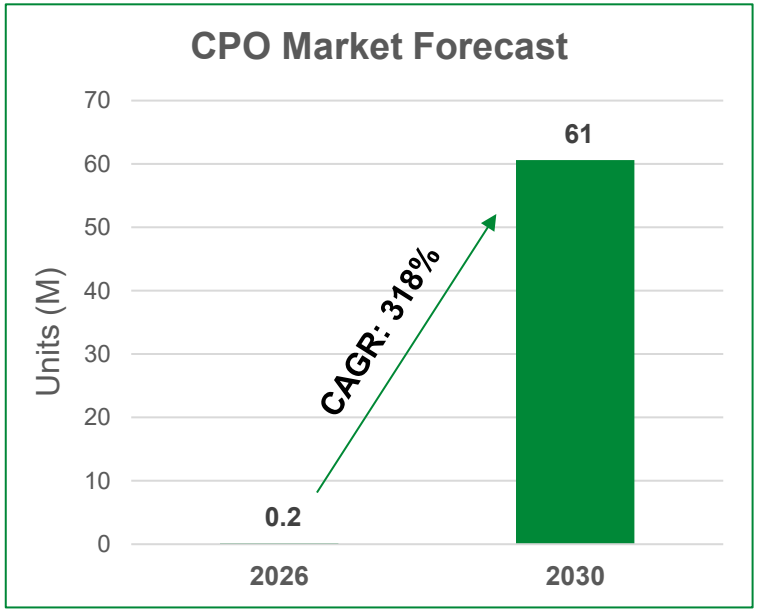



Source: TSMC 2026

- ✓ **Up to 10x greater power efficiency**
- ✓ **Up to 20x lower latency**
- ✓ **Most scalable CPO technology for high volume manufacturing**
  - ➢ Uses same hybrid bonding process technology used currently in logic applications

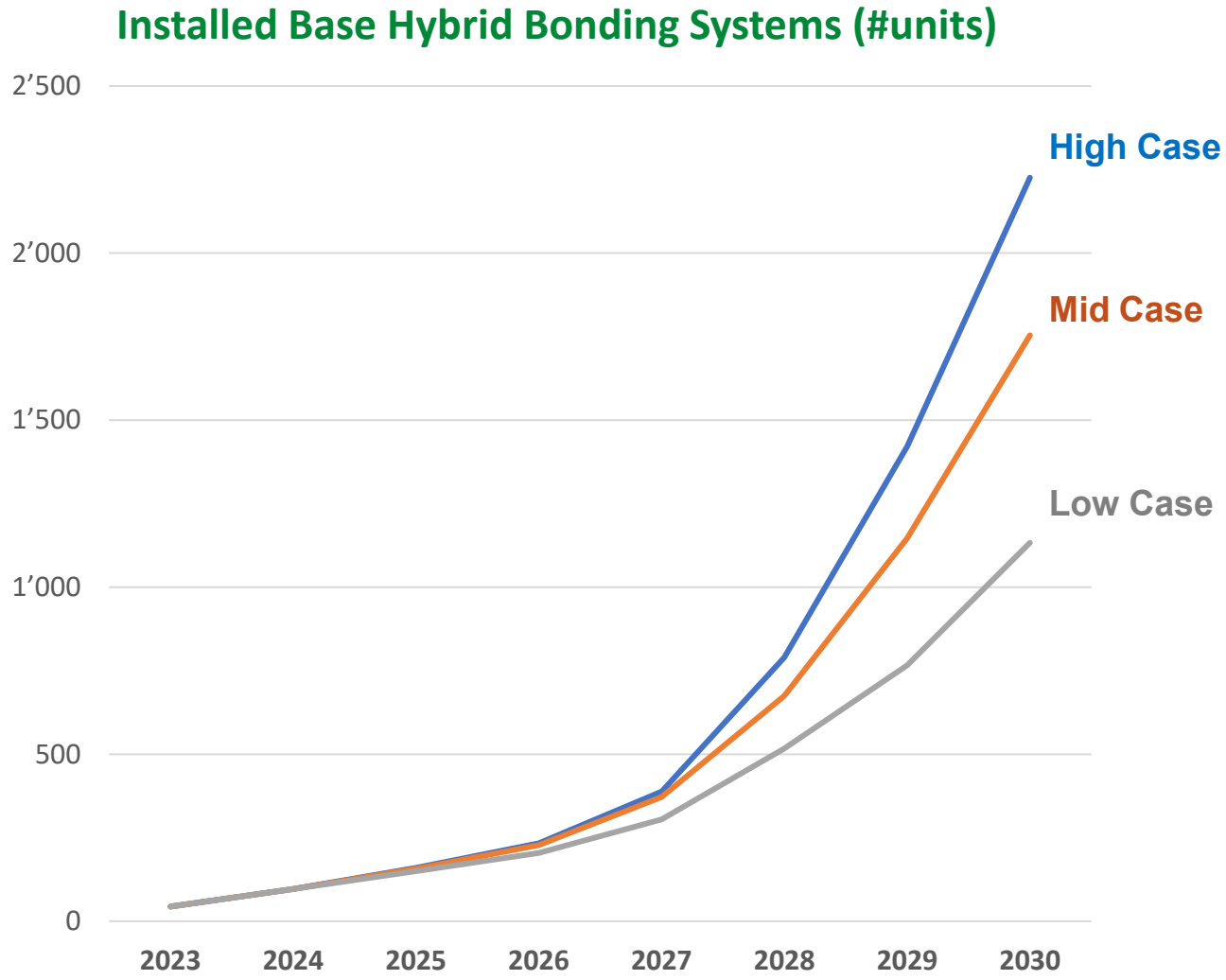
## Significant CPO market growth anticipated

- Should expand hybrid bonding market potential




Source: Lightcounting CPO 2025

# Hybrid Bonding Market Potential Increased Across All Cases




Source: Besi estimates, June 2026

**Estimated 1,150 to 2,200 systems cumulatively by 2030 vs. 960 to 2,000 systems Investor Day 2025**

**Low Case: Logic and CPO applications:**

- **Logic adoption gaining traction**
  - **Intel** launching first hybrid bonded device
  - **Nvidia Feynman** announcement
  - **Apple M5** launch
- **Hybrid CPO** adoption also gaining traction
  - Products now available from **Nvidia** and **Marvell**
- **Cumulative units up 18% from last year's Investor Day**

**Mid case: HBM adoption**

- **Hybrid adoption in memory** estimated to begin in **2027**
  - Starting with **16-high HBM4e stacks**
  - **HBM5 follows next** in with higher HB content
- **Cumulative units up 17% from last year's Investor Day**

**High case: Edge Devices included**

- **Smart phone/tablets**
- Smart Glasses
- **Cumulative units up 12% from last year's Investor Day**

# Fluxless TCB Adoption Increasing For Next-Generation Applications

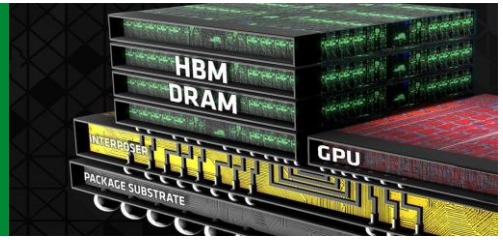
## TC*next* Progress:

- **Customer adoption increased** to 5 customers including memory, logic and CPO producers
- Customer interest expanding (eg: AI logic chips for automotive)

TC*next*

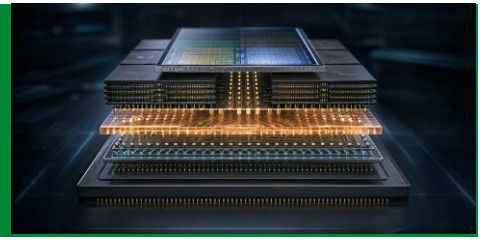
### Memory:

Demonstrated best CoO for TC NCF applications
TC fluxless engagement with a leading customer



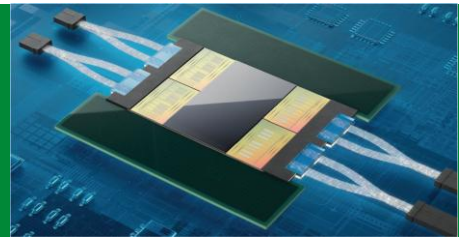

### CoWoS:

"Chip On Wafer" and "On Substrate" interconnect requires fluxless TCB due to increased size of components/interposers



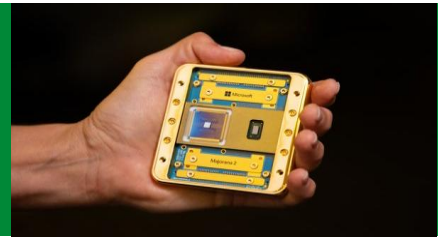
### CPO/LPO/Transceivers:

In addition to hybrid bonding, Fluxless TCB can be used to avoid any contamination of the optical path



### Quantum Computing:

Use of Indium bumps requires fluxless TCB technology with inert environment to avoid oxidation

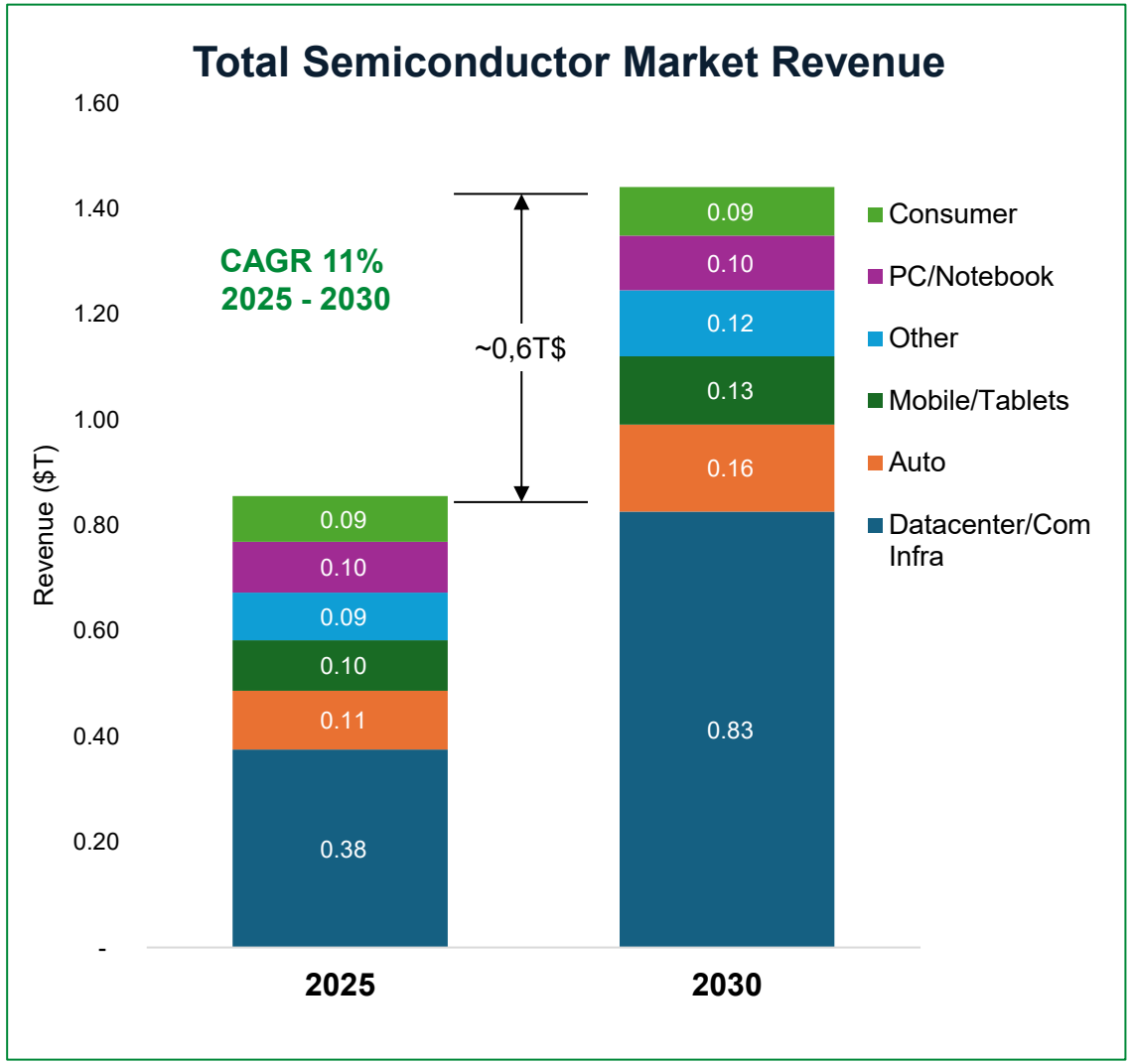


# Wafer Level Assembly Summary

- **Strong Technology Roadmap Extending Besi's Leadership in Hybrid Bonding**
- **Hybrid Bonding Use Cases Confirmed for Logic Applications**
  - Adoption expanding in data center and consumer end markets
  - Significant new use cases announced over past year
- **First Insertion Point for Hybrid Bonding in HBM4e**
  - Customers now preparing for volume manufacturing in 2027
  - Well positioned to capitalize on HBM4E growth opportunity
- **Co-Packaged Optics an Additional Growth Driver**
  - TSMC's COUPE with hybrid bonding is leading CPO technology
  - Offers superior performance, energy efficiency and scalability
- **Hybrid Bonding Market Potential Increased Across All Cases**
- **Applied Materials & Besi Collaboration** Helps Accelerate Hybrid Bonding Adoption and Growth, **2 to 4 Generations Ahead of Competition**
- **Fluxless TCB Adoption Increasing for Next-Generation Applications**


# IV. MAINSTREAM DIE ATTACH
## Christoph Scheiring
## Senior VP Die Attach

# AI Drives Growth In Mainstream Assembly Applications



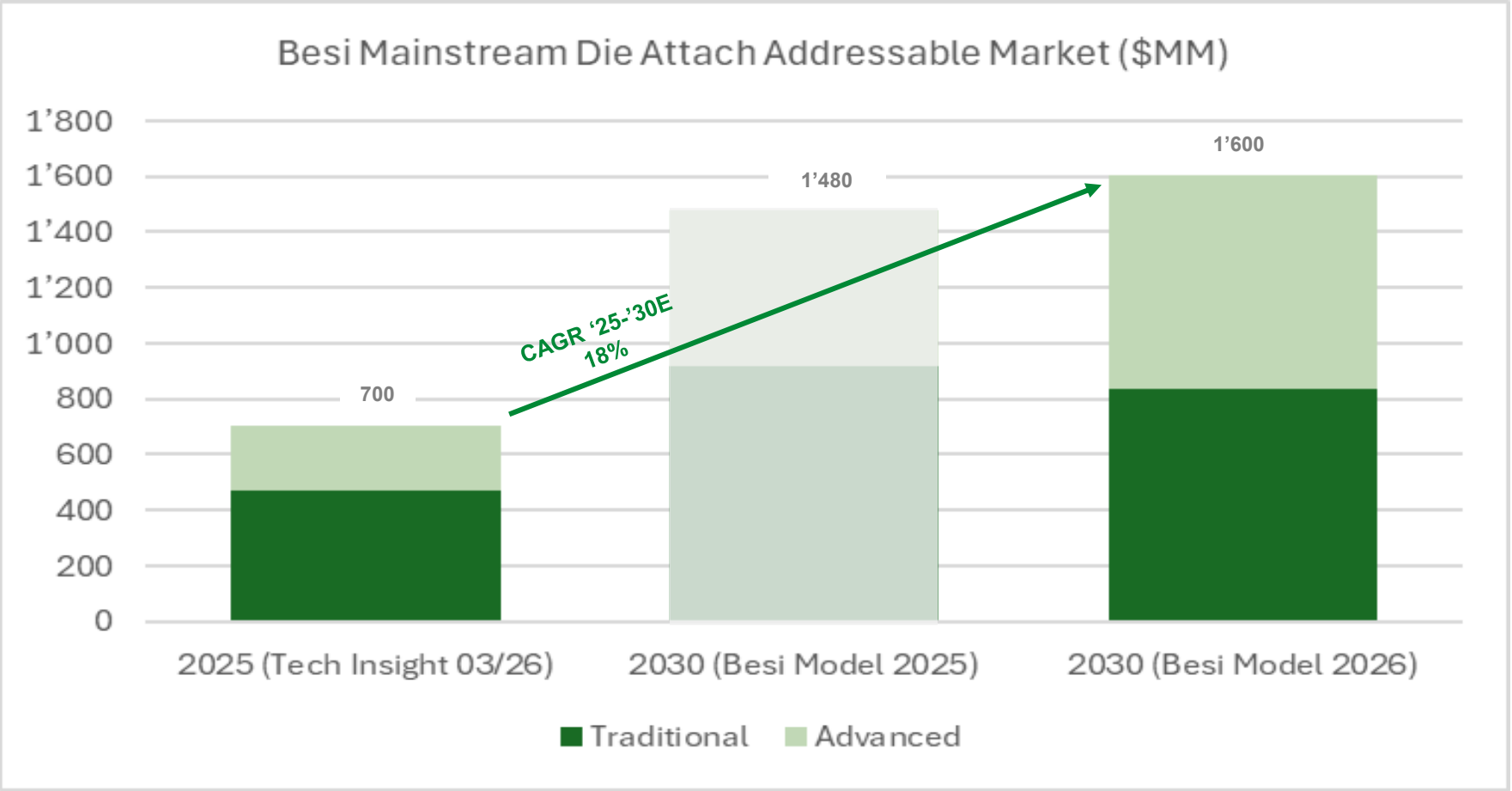

Source: TechInsights 2026

## Key Market Trends

- **AI / Datacenter are primary demand drivers across multiple mainstream applications:** Photonics, 2.5D, Power Management
- **AI also creates demand across Besi's traditional end markets:** AI/data centers, high end smart phones and automotive/power
- **Demand for advanced packaging is accelerating** particularly for high accuracy die attach systems
- **China's AI buildout is another driver** especially given their limited access to the most advanced node sizes

# Besi's Mainstream DA Addressable Market* to Double by 2030

## Besi's 2030E die attach addressable market up 8.1% versus last year's estimate




* Excluding TCB, Hybrid, Die Sorting, LED

Source: Besi / Techinsights June 2026

# Demand Growing Rapidly for Multi-Module and Flip Chip Systems Epoxy and Soft Solder Product Lines Growing More Moderately

Besi

## Multi-module

- **Highest accuracy for photonics and CPO**
- Leading process capabilities for large die AI interposer attach and advanced **camera modules**

## Flip Chip

- **Highest accuracy** C2W (2.5D CoWoS) assembly
- **Highly productive tool of reference** in BGA & CSP & LF flip chip attach
- New tailored **high speed solution** for camera modules

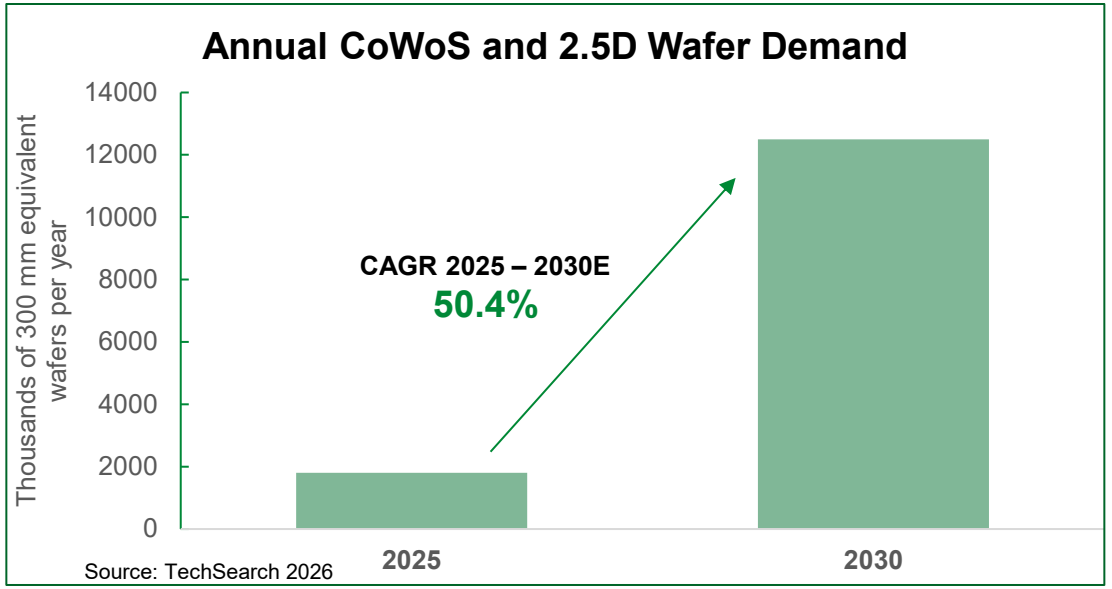
## Soft Solder

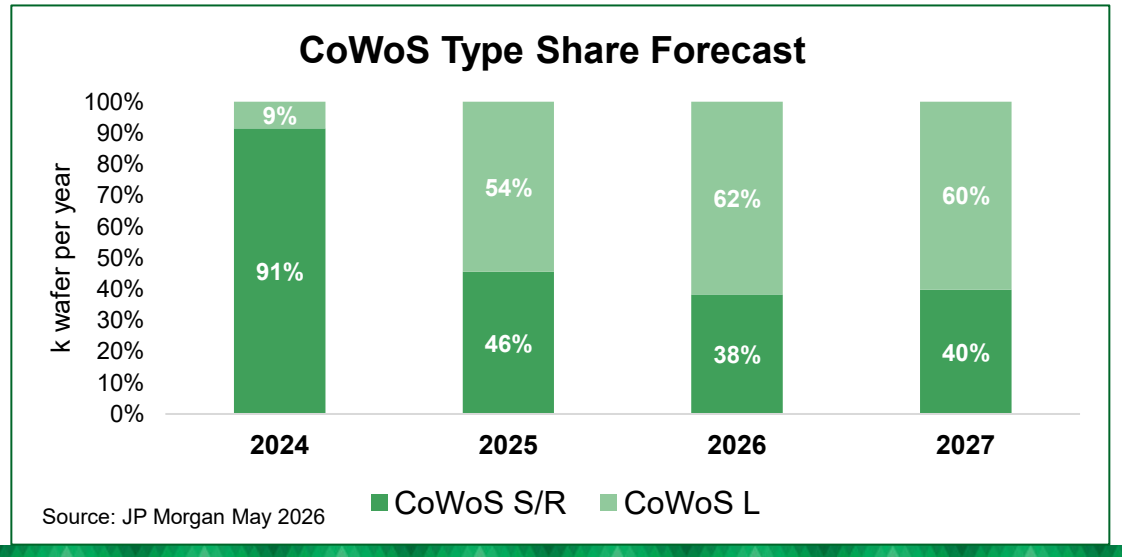
- **Leading soft solder process** (oxygen level, gas consumption) for **automotive power** applications
- Unique diffusion solder process offering

## Epoxy

- **Industry leading accuracy and speed in epoxy die attach**
- Stringent epoxy control for mobile and automotive power and sensor applications

# Strong 2.5D Packaging Unit Growth Together with Increased Die Attach Intensity Drives Advanced Packaging Equipment Growth




## 2.5D Key Market Trends

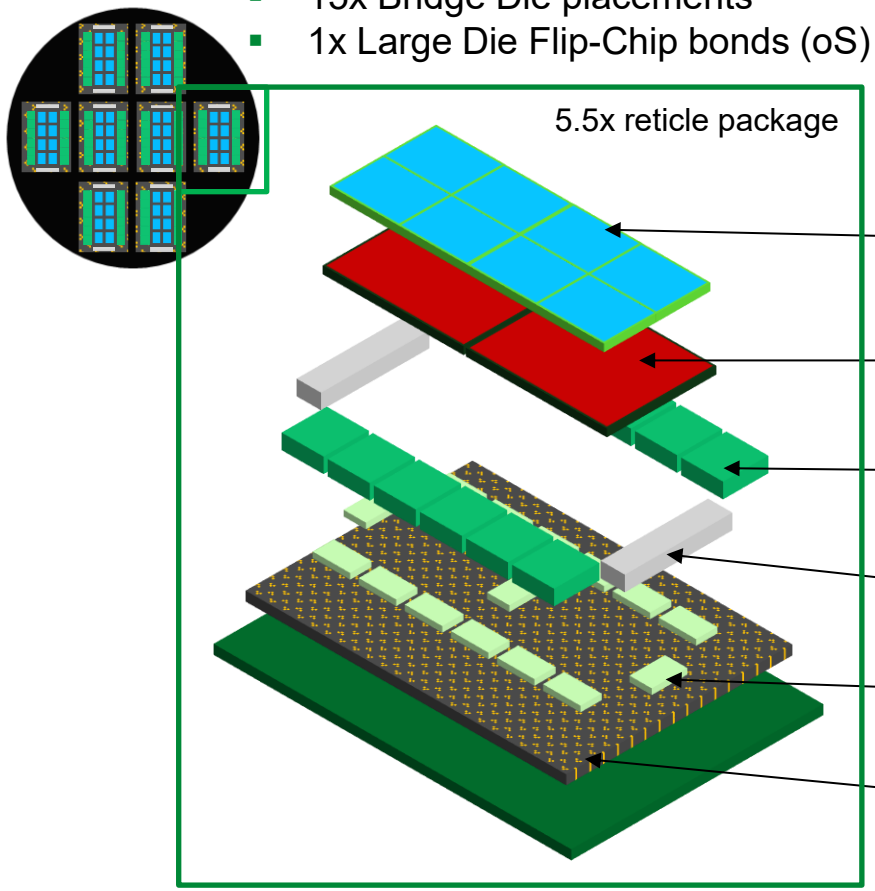
- **2.5D wafer demand** expected to grow by **50.4% CAGR** driven by growth in **AI accelerators** and **datacenter processors**
- **Number of die attach steps per device is increasing**
  - Die sizes increasing as Moore's Law scaling slows
  - 2.5D packaging platforms evolving to support more dies per package and larger package sizes
  - **CoWoS-L** emerging as dominant architecture. Requires additional embedded bridge dies.
- **Panel level assembly** (e.g. CoPoS) in development due to increased package sizes

# Multiple Growth Opportunities in 2.5D Advanced Packaging

## Next Generation Accelerator Package Structure

Each Module contains:

- 8x Hybrid bonds (SoIC)
- 16x Flip-chip bonds (2x 3DIC, 12x HBM, 2x IO)
- 15x Bridge Die placements
- 1x Large Die Flip-Chip bonds (oS)




**Besi's 2.5D participation is expanding with new platform introductions**

**8800 CHAMEO HB**

Hybrid Bonding

**NEW 8800 Chameo *Flex***

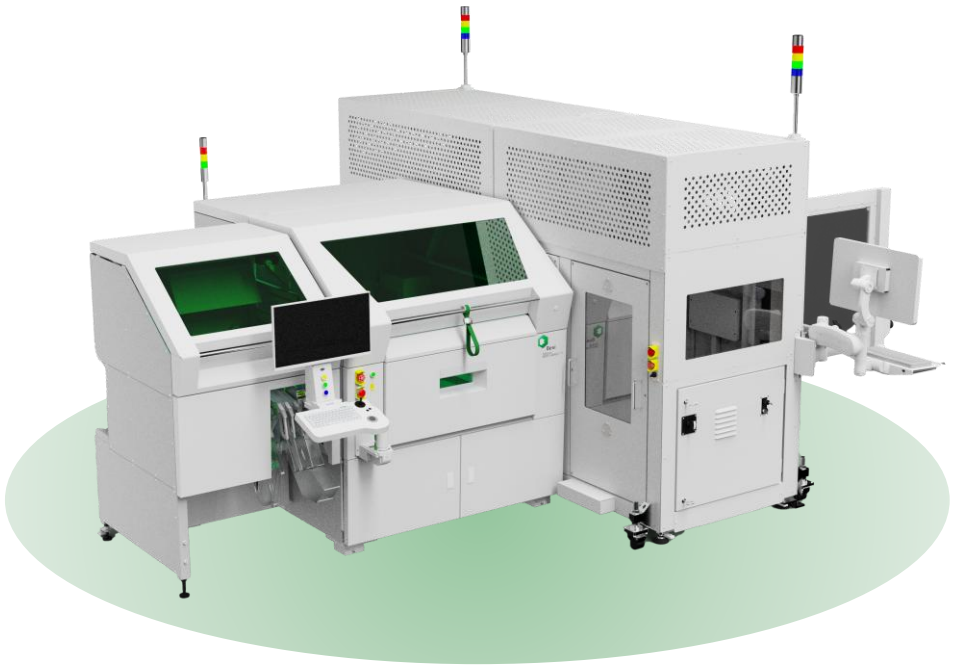
**NEW 8800 TC Next**

Flip-chip, TCB & Bridge Die Attach

**2200 evo**

Large Die Interposer Attach

# 8800 CHAMEO *fleX* – New Flip-chip & Bridge Attach Platform Expands Share in 2.5D Packaging with Highest Accuracy, Speed and Flexibility



## Key Competitive Advantages

- ✓ **Highest Productivity:** CoW / CoPanel 4000 uph
- ✓ **Best-in-class Accuracy:** 1µm
- ✓ **Broad application range:** IC, HBM, Bridge die
- ✓ Combining Front & Back End **Automation**
- ✓ **Ready for Panel** 310 x 310 mm

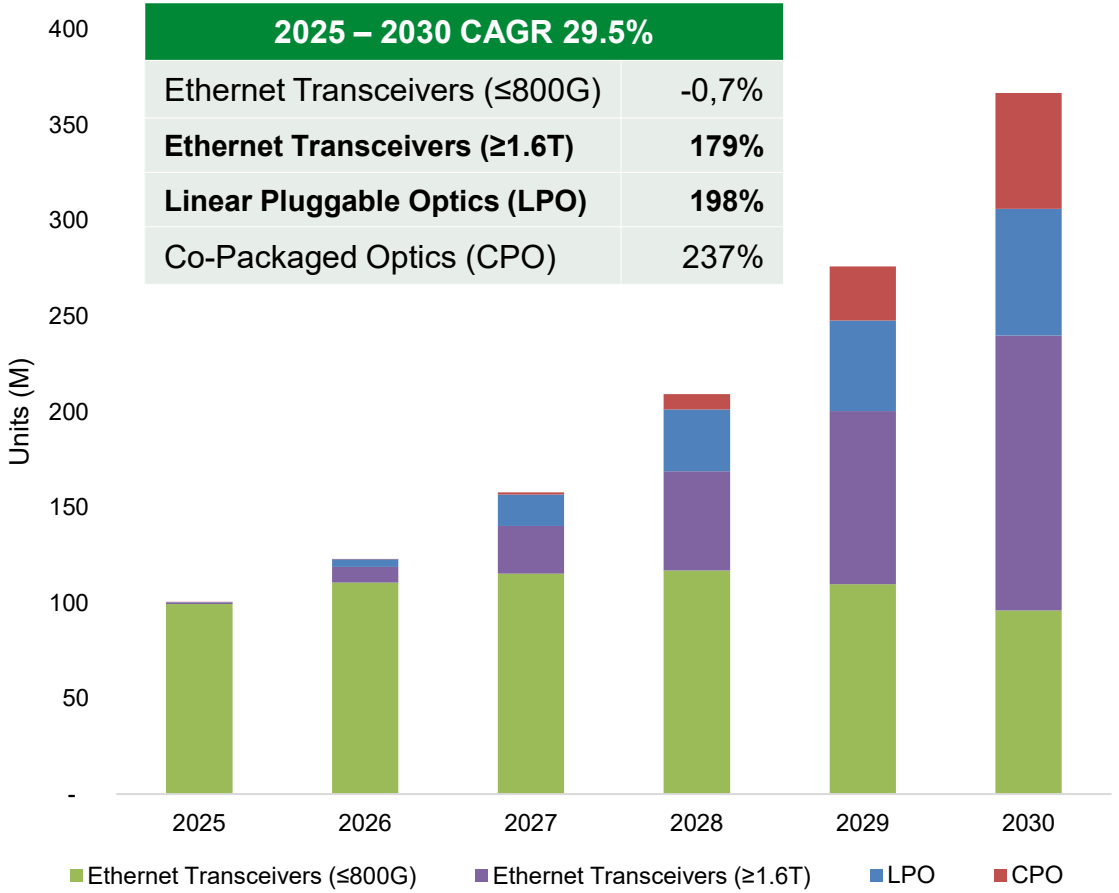
## Gaining Customer Traction

- **Introduced Q4 2025** – strong customer interest
- 1st Qualification **completed successfully**
- Building on success of Besi's industry leading **8800 Chameo** Advanced C2W flip-chip system
- Targets significant growth in 2.5D capacity by foundries and OSATs
- **Active Engagement** with 3 major IDMs and 4 major subcons

# Photonic Solutions for AI Data Centers is Another Rapidly Growing Market Opportunity

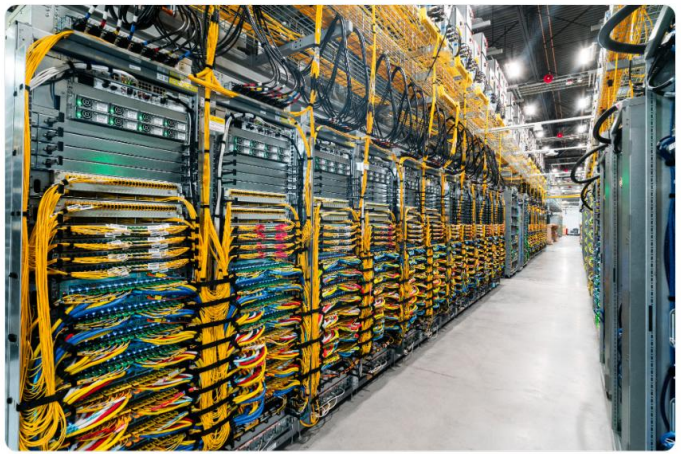
## Optical Interconnect Forecast

| 2025 – 2030 CAGR 29.5% | |
|---|---|
| Ethernet Transceivers (≤800G) | -0,7% |
| **Ethernet Transceivers (≥1.6T)** | **179%** |
| **Linear Pluggable Optics (LPO)** | **198%** |
| Co-Packaged Optics (CPO) | 237% |




Source: LightCounting Oct. 2025

## Data centers utilize millions of photonic transceivers to connect servers and racks over optical fiber



Source: Google

Pluggable optical transceiver

Source: Nvidia

## Photonics Market Trends

- Optical interconnect market growing by **29.5% CAGR**
- Rapid technology shift to **1.6T transceivers**
- Demand for LPO (Linear Pluggable Optics) increasing to address power constraints in AI factories
- Besi market share gains anticipated

# Besi's Multi Module Attach System: Leading Photonics Platform in Rapidly Growing Market

## Besi # 1 vendor, engagement with all key players

**2200 Evo advanced**

**2200 Evo ONE**

**Industry leading system** for various **transceiver** assembly steps (800G, 1.6T, LPO)
- 3 µm accuracy
- 325 x 200 mm substrate

Introducing **new Evo platform** to **expand addressable market**
- 1um accuracy
- 300 mm wafer capability
- Eutectic bonding capability
- Customer evaluations in progress

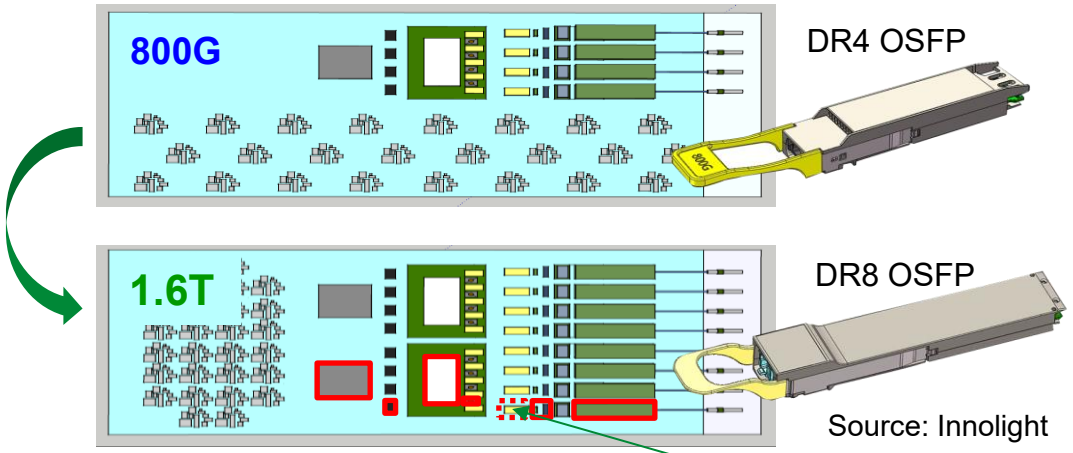
NVIDIA fabrinet molex eoptolink COHERENT

INNO LIGHT FINISAR Accelink HG Semiconductor Limited 宏光半導體有限公司

## Significant Growth Opportunity

- **Die attach intensity increasing**
  - 1.6T transceivers increasing #die attach steps (more of the same processes per transceiver)
- **Increasing addressable share of transceiver market**
  - Leveraging Evo ONE platform to address additional transceiver process steps

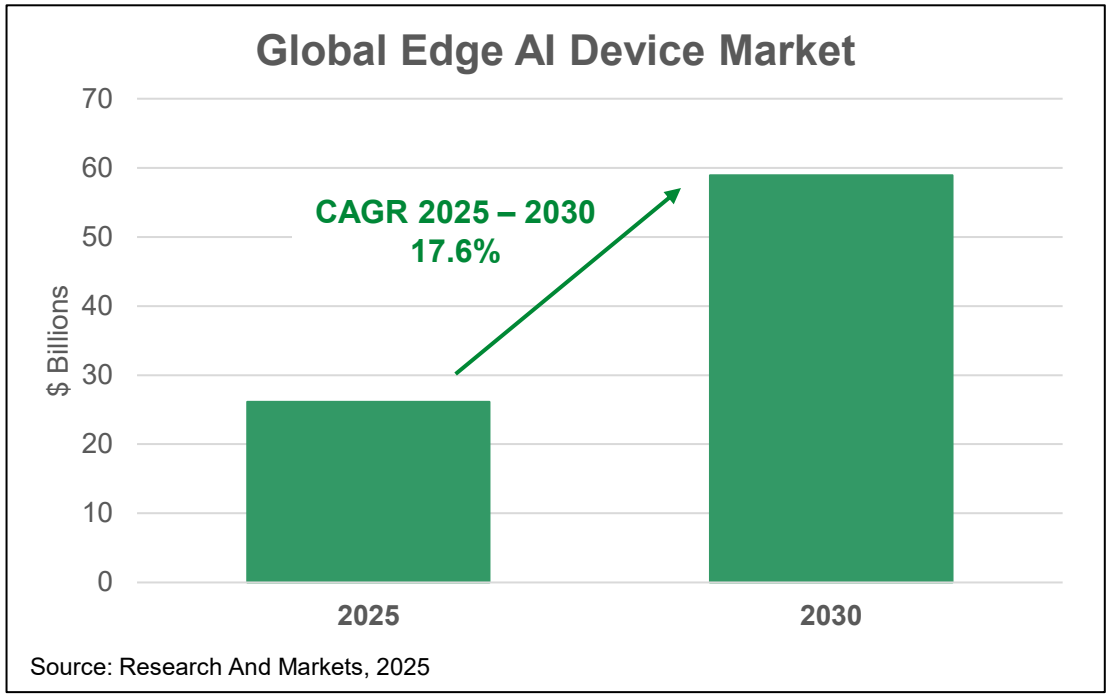
**1.6T Transceivers require up to 2x number of die attach steps**




Source: Innolight

BESI process steps DSP, PD, TIA, LD, IS, FAU, **New:** Laser

# Besi Die Attach Solutions Preferred Choice for Edge AI Semiconductor Applications



Source: Research And Markets, 2025

- **Edge AI Device Market expanding at 17.6% CAGR** driven by demand for real-time processing and enhanced privacy
- **Smartphones dominating Edge AI market** for the foreseeable future
- **Robotics, Automotive and AR/VR Eyewear** are emerging applications

## AI Compute Moves on Device

- **Increasing use of Edge AI devices, particularly smartphones**
  - **Higher semiconductor content** driven by increased functionality (AP, memory, sensors)
  - **New camera applications** (mechanical aperture and others)

**Besi Mainstream Die Attach Solutions Well Aligned With Edge AI Device Requirements**

**2200 evo**

**Application Drivers**

- Smartphone camera
- AR/VR devices

**2100 hSi / SSI / FC**

**Application Drivers**

- RF Power amplifiers
- Sensors
- Power Mgt ICs

**8800 FCQ / Chameo / CIS**

**Application Drivers**

- Processors
- Memory
- Camera

# Mainstream Die Attach Summary

- **AI structural growth driver** across **broad range of end markets** and **Besi's product portfolio**
- **Increasing Die Attach Intensity** creates multiplier effect on **equipment demand**
- Besi's mainstream die bonding **addressable market expected to more than double** by 2030
- **Increasing 2030 revenue model by 10%** vs. last year's Investor Day
- **Favorably positioned** in highest growth segments of advanced packaging:
  - 2.5D/CoWoS
  - Photonics
  - Edge AI Devices
- **New product introductions well on track**
  - Expected to accelerate growth and increase market share

# V. Summary
# Richard Blickman
# CEO

# Target Model Update

| Current Target | | New Target |
|---|---|---|
| € 1.0 billion | Engine 1 Revenue | € 1.1 billion |
| € 0.5-0.9 billion | Engine 2 Revenue | € 0.6-1.1 billion |
| 40%+ | Addressable Market Share | 40%+ |
| 64-68% | Gross Margin | 64-68% |
| 40-55% | Operating Margin | 45-55% |
| Net Zero GHG by 2030 | Scope 1 & 2 Emissions | Net Zero GHG by 2030 |
| 100% from renewable sources | Global Energy Needs | 100% from renewable sources |

**Increasing Besi's long term revenue model to range of € 1.7 – € 2.2 billion**

- **Up ~15%** at midpoint
- Increasing **Engine 1 (Traditional Advanced Packaging)** revenue target by **10%**
- Increasing **Engine 2 (Submicron Accuracy)** revenue target by **~21**% at midpoint

**Increasing operating margin to range of 45%-55%**

- Other targets remain unchanged

# CEO Summary

| | |
|---|---|
| ✓ | Overall WFE & assembly **outlook significantly improving** due to AI infrastructure build |
| ✓ | **Industry conditions have moved from surplus to deficit** and unit growth has accelerated |
| ✓ | **Besi well positioned** with leading market shares in its addressable markets |
| ✓ | New Besi **upcycle began in H2-25** |
| ✓ | **Revenue, orders and profitability have accelerated** since Q2-25 |
| ✓ | Significant **progress achieved on long term plan realization** |
| ✓ | **Multiple drivers converging** to accelerate **hybrid bonding growth** |
| ✓ | **Increasing 2030 revenue and operating margin targets** |
| ✓ | **Adjusting operating model** in alignment with growth potential |

# VI. Q&A

# Investment Considerations

Besi

- Assembly market ever more critical in semiconductor value chain
- Disciplined strategic focus has created an industry leader
- Long term secular trends drive advanced packaging growth
- Wafer level assembly for AI applications promising new growth opportunity
- Market presence has grown via key IDMs, supply chains and partners
- Tech leadership and scalability result in superior financial returns
- Commitment to sustainable growth and fighting climate change
- Attractive capital allocation policy