INVESTOR DAY PRESENTATION

June 6, 2024

Safe Harbor Statement

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward looking statements, which are found in various places throughout the presentation, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward looking statements, although not all forward-looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward-looking statements. While these forward looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 and other global pandemics, and the associated adverse impacts on the global economy, financial markets, global supply chains and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; consolidation activity and industry alliances in the semiconductor industry that may result in further increased customer concentration, inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, conflict minerals regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region where we have a substantial portion of our production facilities; potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel, including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers; those additional risk factors set forth in Besi's annual report for the year ended December 31, 2023 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.

Agenda

I.	Strategic Overview	Richard Blickman
II.	Market Trends	Chris Scanlan
III.	Wafer Level Assembly	Peter Wiedner
IV.	Mainstream Die Attach	Christoph Scheiring
V.	Q&A	Besi Team

I. STRATEGIC OVERVIEW
Richard Blickman
CEO

CEO Summary

AI Drives New Era of Advanced Packaging

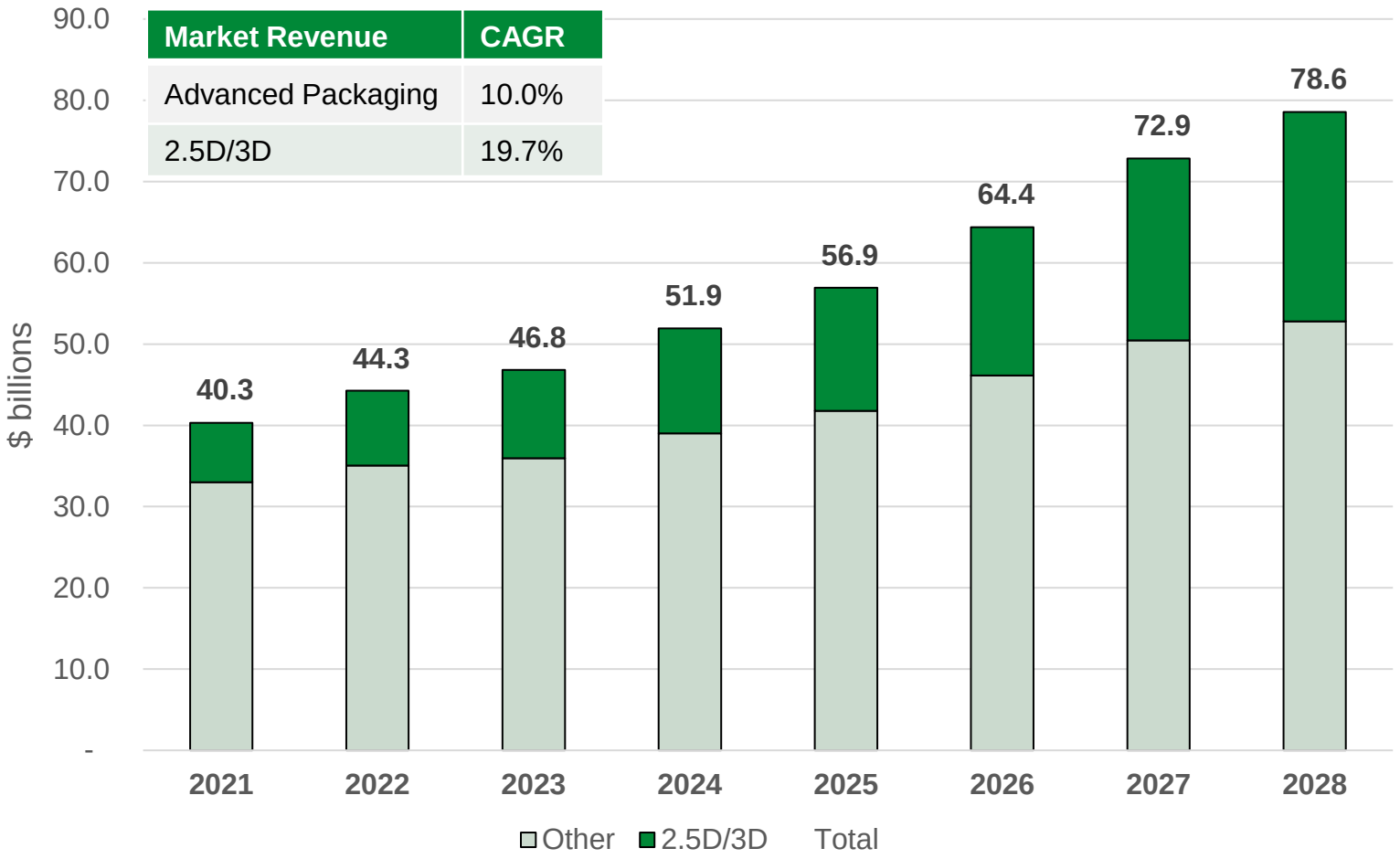
- Use of Generative AI accelerating everywhere
- Assembly one of major gating items to realize AI promise and extend Moore's Law
- In very early stages. New device architectures/applications still evolving
- ~35-40% of Besi's orders currently from AI related applications

Use of Both 3D and 2.5D Assembly Structures Facilitate AI Growth

- Major logic players now in commercial production of 3D hybrid bonded devices
  - Adoption spreading to memory manufacturers. Anticipated ramp 2026-2027
- Orders for 2.5D capacity began on larger scale in H2-23
  - Particularly for CoWoS and photonics assembly
- Memory customers pursuing dual 2.5D/3D strategy in face of rapid AI adoption and significant HBM demand
- Besi further expanding R/D to provide complete AI assembly solutions for customers

Advanced Packaging Revenue Forecast to Grow Rapidly 2.5D/3D Fastest Growing Segment

Market Revenue	CAGR
Advanced Packaging	10.0%
2.5D/3D	19.7%



Source: Yole. November 2023

Besi Portfolio Well Positioned by Node Size and Accuracy

- 70% of Besi equipment revenue defined as advanced packaging
- 50% equipment revenue advanced die placement (< 7 micron accuracy)

CEO Summary - Continued

Mainstream Assembly Market Slow to Recover Post Pandemic

- 2+ years industry downturn
- Continued weakness in smartphone, automotive and consumer applications
- Despite increased utilization rates generally
- Expected H2-24 improvement

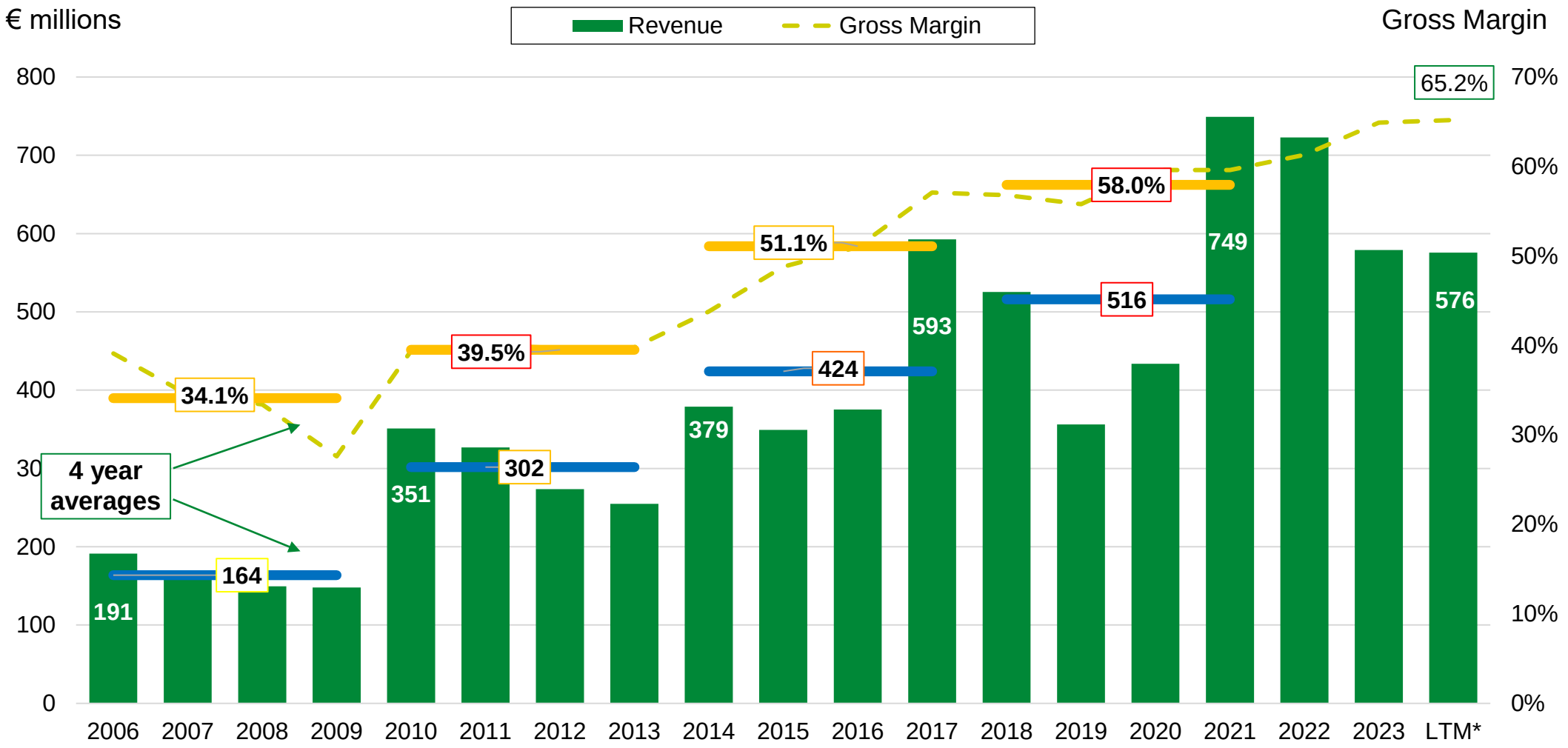
Strong Performance in Downturn

- Revenue, orders and operating profit up 62.5%, 57.2% and 132.2% vs. last cycle
  - Operating margin up 11.1 points
- Addressable market share has increased in key die attach and packaging markets
- Record capital allocation of € 435.5 million in 2023. € 196.4 million YTD 2024

Well Positioned for Next Industry Upturn

- Best in class advanced packaging portfolio
- Market moving to sweet spot of core technological competencies
- Multiple drivers of growth: AI, mainstream recovery and onshoring of capacity
- Business model revenue targets intact. Capacity and personnel in place

Besi's Step Function Growth Through Cycles



* LTM including midpoint of guidance for Q2-24

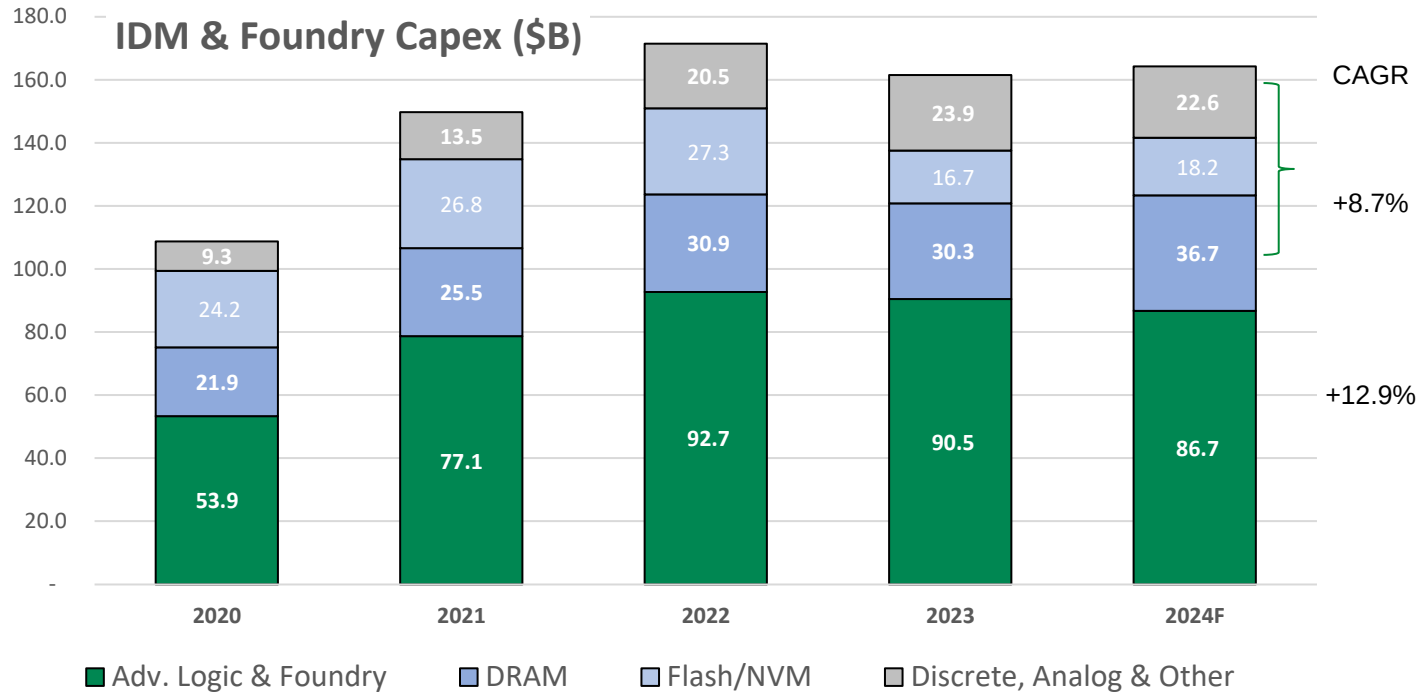
Semi Cap Equipment: Limited Recovery Expected in 2024. Pockets of Growth in AI and Memory

TOP IDM & FOUNDRY CAPEX SPENDERS

(Capital expenditures by company, $B, ranked by 2024 Forecast)

	2020	2021	2022	2023	2024F
Samsung	28.1	38.0	36.6	37.0	35.5
TSMC	17.2	30.0	36.3	30.5	30.1
Intel	14.3	18.7	23.7	25.0	26.2
SK hynix	8.4	10.9	13.9	6.4	9.6
Micron Technology	8.8	10.2	11.2	6.3	8.3
SMIC	5.7	4.5	6.4	7.5	7.4
CXMT	2.5	2.9	2.6	6.1	6.0
Texas Instruments	0.6	2.5	2.8	5.1	5.0
XMC/YMTC	2.9	3.1	3.0	3.5	3.4
Infineon	1.1	1.6	2.3	3.0	3.1
UMC	1.0	1.8	2.7	3.0	3.3
KIOXIA/WD	3.5	5.4	2.8	2.2	3.0
Sony	2.4	2.6	2.9	3.4	3.7
STMicroelectronics	1.3	1.8	3.5	4.1	2.5
GLOBALFOUNDRIES	0.6	1.8	3.1	1.9	0.7
Huahong Group	2.2	1.9	1.0	1.2	1.4
Nexchip	0.8	0.8	0.7	0.7	0.6
Others	7.4	11.1	15.8	14.8	14.3
Total	108.7	149.7	171.4	161.5	164.2
y-o-y growth	*12%*	*38%*	*14%*	*-6%*	*2%*
Top 3 (% of Total)	55%	58%	56%	57%	56%
Top 5 (% of Total)	71%	72%	71%	66%	67%

Source: Tech Insights, May 2024



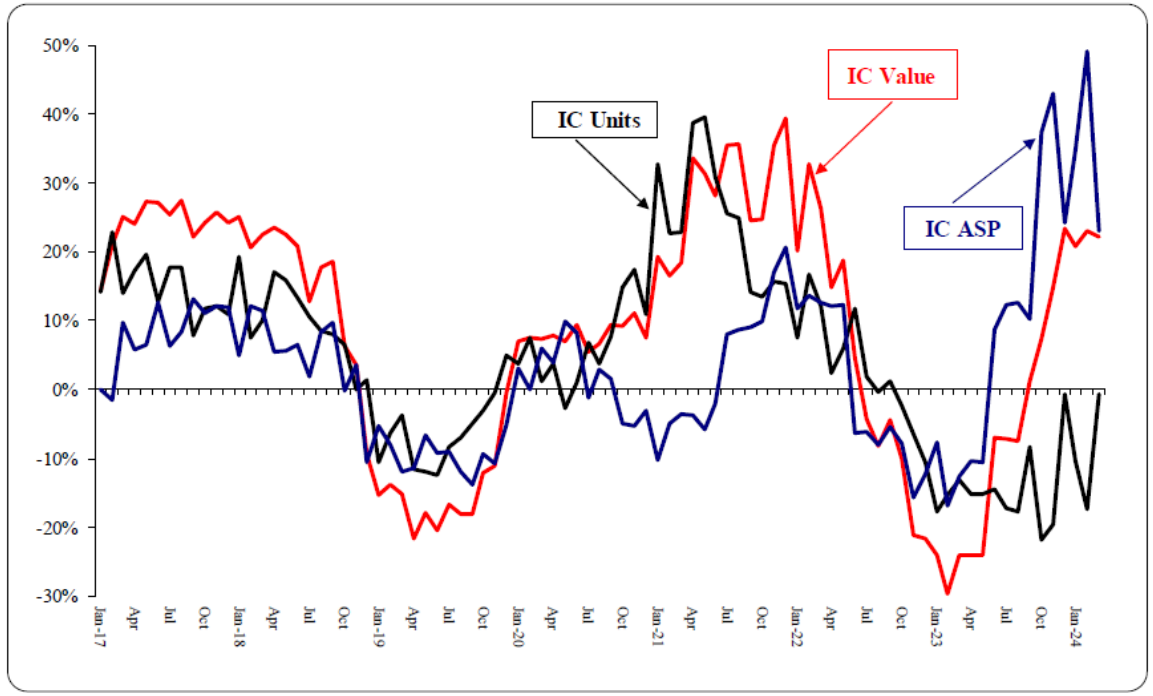
2023 Semi capex decrease driven by top 5 producers (12.6%)

2024E Semi capex forecast to increase by 2% to € 164 billion

- Driven by top 5 producers: +4.3%
- Mostly for memory applications

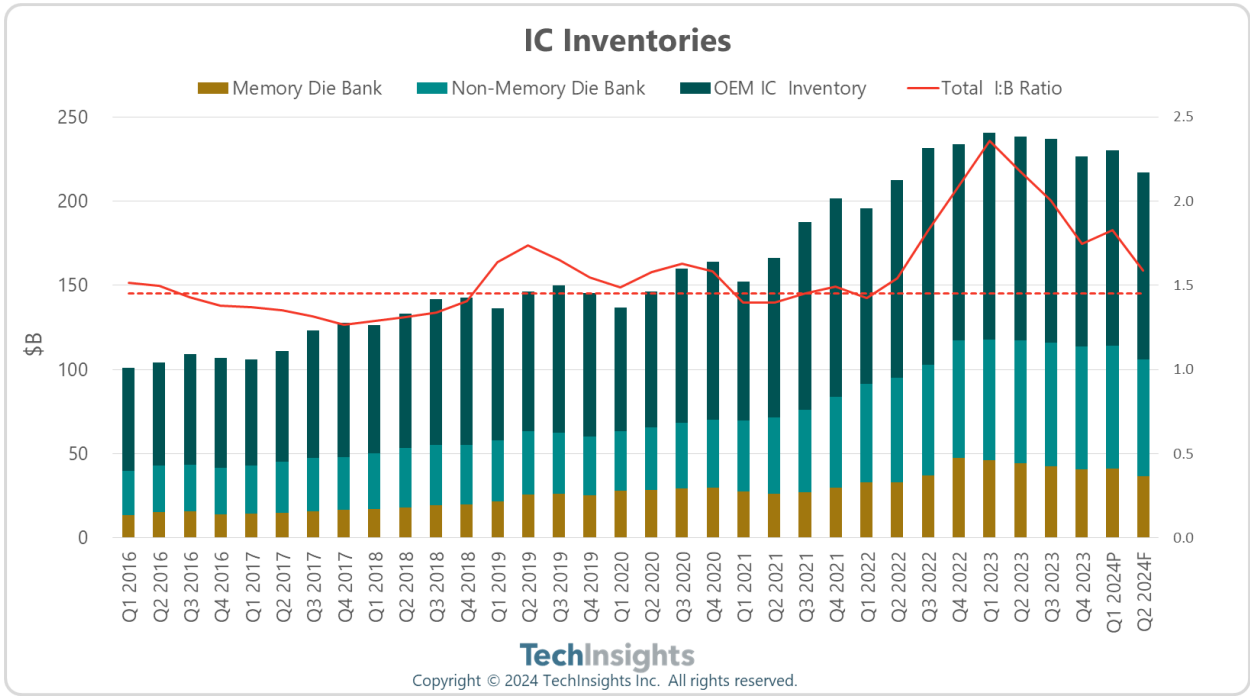
IC Unit Volume in Downturn Since Q3-22
Inventory Levels Declining but Still Elevated

Worldwide IC Annual Growth Rate Unit & Value (Jan 2017 – Mar 2024)



Source: WSTS/Future Horizons (Growth rates adjusted for 5-week months)

IC Inventories (Q1 2016 – Q2 2024)



Significant New Fab Investments Planned Globally Aided by State Funding

Key Front End Fab Projects	Initiated	Cost ($B)	Status
TSMC 3nm - Tainan, TW	2021	60	In progress
TSMC – Arizona, USA	2021	65	In progress
TSMC 2nm - Hinschu, TW	2022	40	In progress
TSMC 2nm - Kaohsiung, TW	2023	26	In progress
Intel - Ohio, USA	2022	28	In progress
Intel Fab 38 - Kiryat Gat, Israel	2022	28	In progress
Intel Fab 52 & 62 - Arizona, USA	2021	32	In progress
Samsung - Taylor, TX	2022	45	In progress
Samsung - Pyeongtaek, South Korea	2022	34	In progress
SK Hynix DRAM - Cheongju, South Korea	2022	11	In progress
Micron DRAM – Idaho, USA	2022	15	In progress
Micron DRAM - New York, USA	2024	30	In progress
Texas Instruments - Texas, USA	2022	30	In progress
Texas Instruments - Lehi, UT	2023	11	In progress

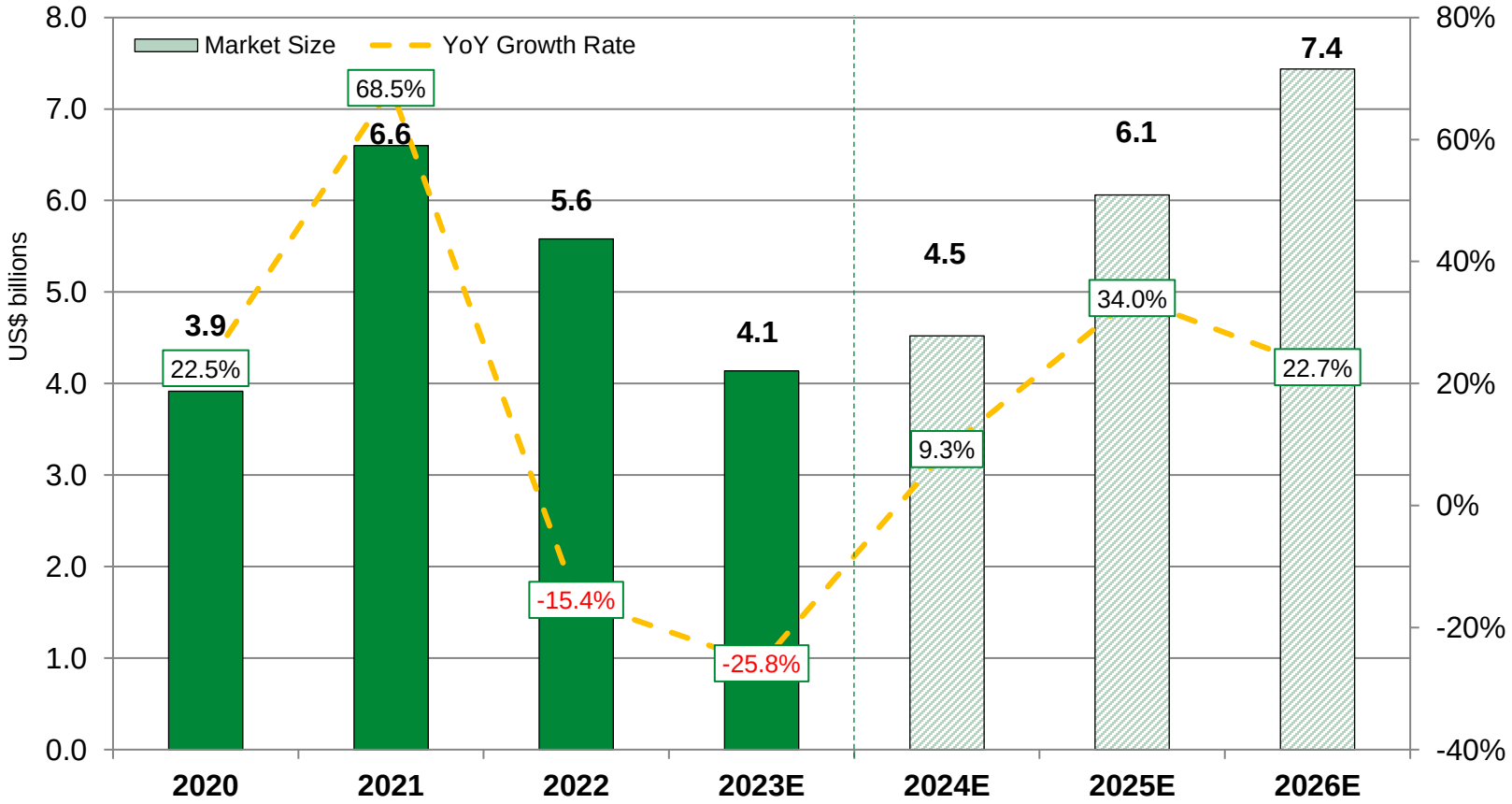
Packaging Fab Projects	Initiated	Cost ($B)	Status
TSMC CoWoS & SoIC - Chiayi, Taiwan	2024	15	In progress
Intel - Penang, Malaysia	2022	7.1	In progress
Intel Fab 9 & 11x - New Mexico, USA	2021	4.0	Ramping
Intel - Wrocław West, Poland	2023	4.6	Planned
Amkor Technology – Arizona, USA	2024	2.0	Planned
Micron - Gujarat, India	2023	2.8	In Progress
Micron - Xi'an, China	2023	0.6	In Progress
Samsung - Texas, USA	2024	4.0	Planned
SK Hynix M15 Expansion - South Korea	2024	1.0	In Progress
SK Hynix HBM - Indiana, USA	2024	3.9	Planned
SPIL P1 - Pulau Pinang, Malaysia	2024	1.3	In Progress
Tata TSAT - Assam, India	2024	3.2	Planned
Silicon Box - Italy	2024	3.6	Planned
JCET (automotive) - Shanghai, China	2023	0.2	In Progress

Government Funding of Semiconductor Capacity/R&D Exceeds US$200 B

US Chips Act	EU Chips Act	China Big Fund	South Korea	Japan	Taiwan	India	Malaysia
$52.7B Initiated 2022 Includes $11B R&D	**$46.5B** Initiated 2023 Includes $3.1B R&D	**$27B** (phase 2) Initiated 2019 New **$47.5B** round announced	**$19.7B** Initiated 2022	**$13.9B** Initiated 2021	**$16B** Initiated 2023	**$10B** Initiated 2021	**$5.6B** Announced May 30, 2024

Source: TechInsights, Besi

Assembly Equipment Market Recovering Slowly. Growth Anticipated to Accelerate in 2025/2026



2024 growth revised downwards reflecting slow mainstream recovery

- 2024 forecast expects 9.3% increase
  - Down from original forecast of 31%
  - Driven by AI

Market expected to recover strongly in 2025/2026

- Forecast $ 7.4 billion in 2026
  - +80% from 2023 levels

Secular fundamentals intact:

- AI, Datacenter, HPC, 5G, primary drivers
- Investment in new process technologies: hybrid bonding/CSP
- Onshoring new advanced packaging fabs

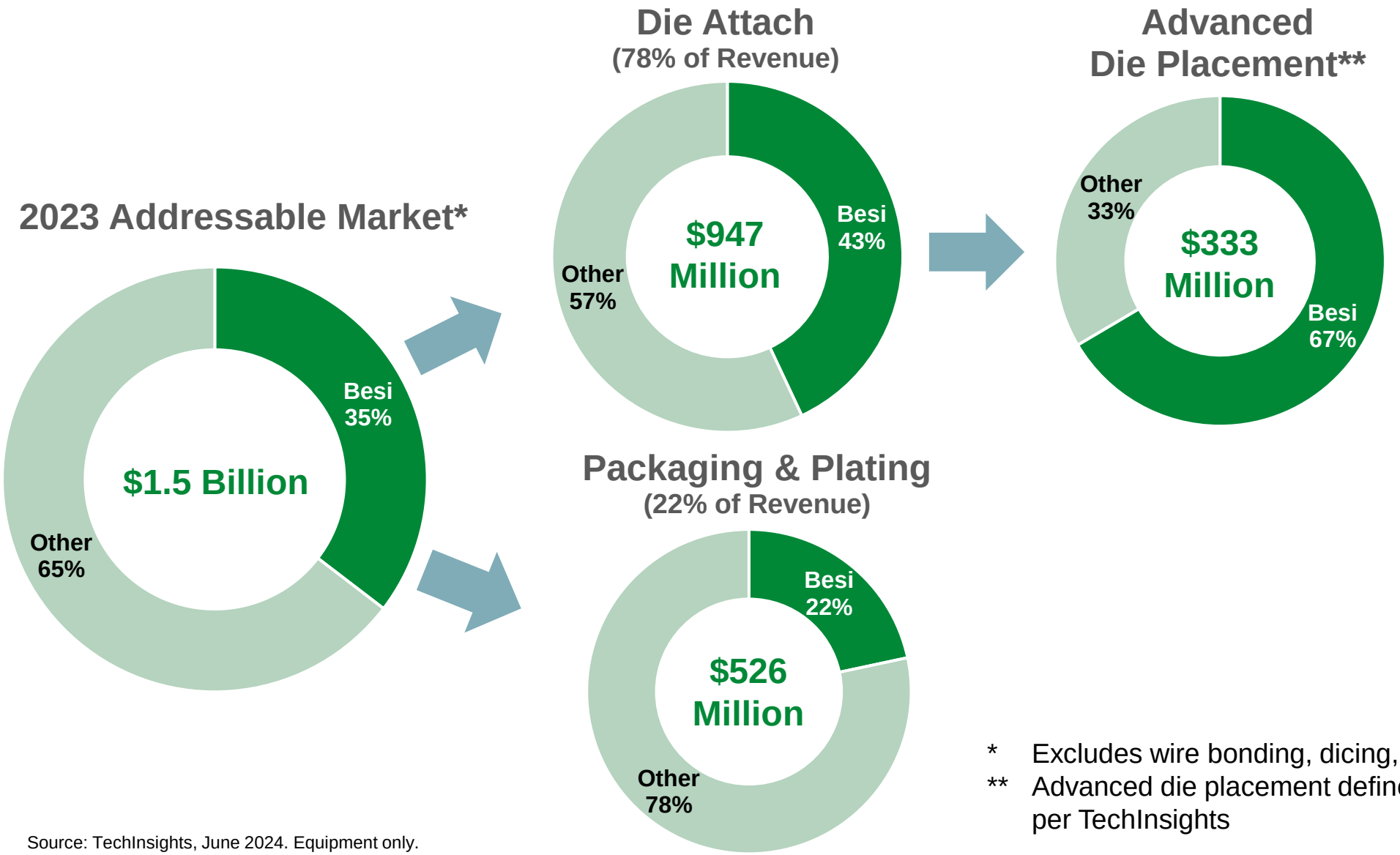
Source: TechInsights, June 2024. Assembly equipment revenue excludes service revenue.

Besi Addressable Market Share Increasing Particularly in Key Die Attach Markets

	2019	2020	2021	2022	2023	Δ '23/'22	Δ '23/'19
Assembly Market ($MM)	3,197	3,916	6,635	5,578	**4,139**	-25.8%	+29.4%
Besi Market Share	10.1%	10.5%	11.7%	11.4%	**12.6%**	**+1.2pts**	**+2.5pts**
Addressable Market ($MM)	1,257	1,439	2,484	2,000	**1,473**	-26.4%	+17.2%
Besi Market Share	25.7%	28.5%	31.2%	31.7%	**35.4%**	**+3.7pts**	**+9.7pts**
Die Attach	30.6%	35.4%	38.9%	38.7%	**43.0%**	**+4.3pts**	**+12.4pts**
Packaging & Plating	16.8%	15.3%	15.4%	18.3%	**21.6%**	**+3.3pts**	**+4.8pts**
% of Besi Revenue	**2019**	**2020**	**2021**	**2022**	**2023**		
Die Attach	76%	82%	82%	80%	**77%**		
Packaging & Plating	24%	18%	18%	20%	**23%**		

Source: TechInsights, June 2024

Leader in Addressable Market, Die Attach Market and Advanced Die Placement



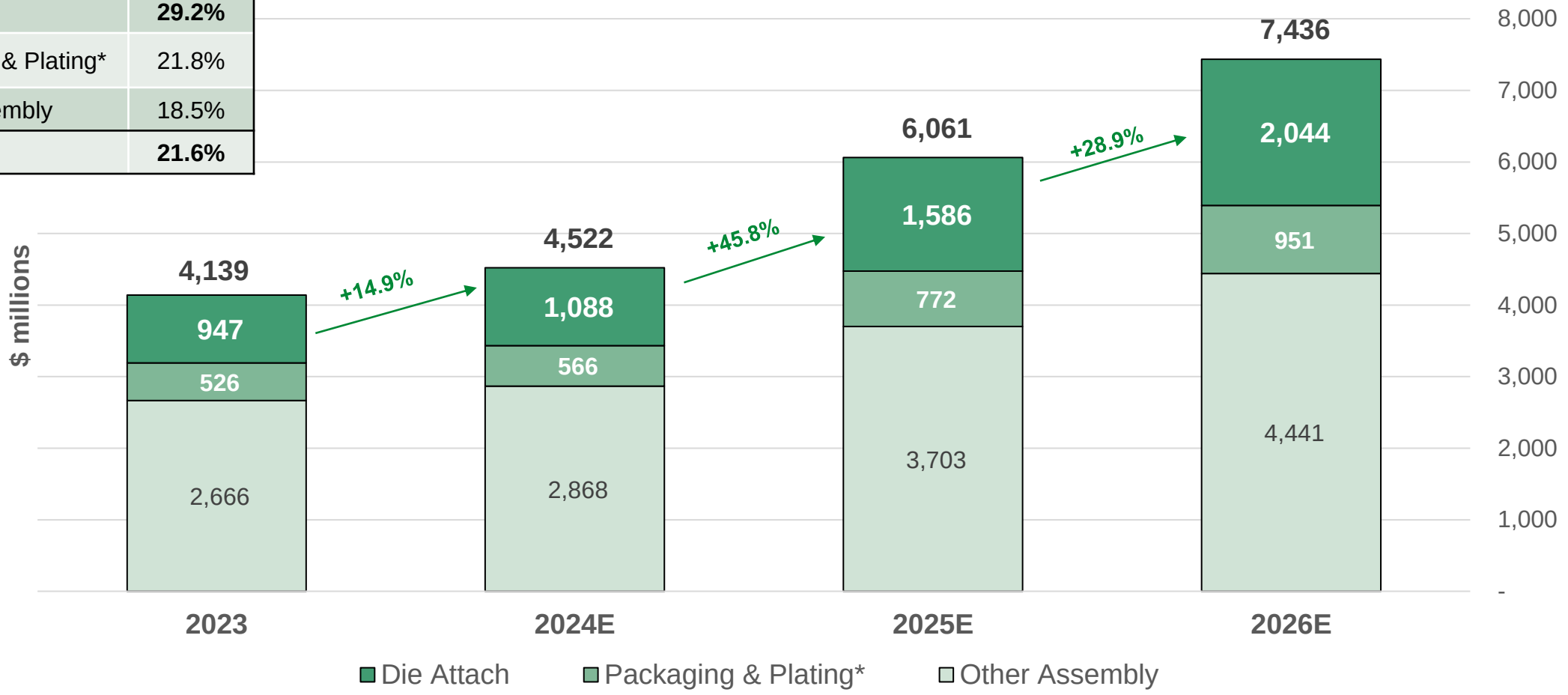
Source: TechInsights, June 2024. Equipment only.

* Excludes wire bonding, dicing, and other.

** Advanced die placement defined as < 7 micron accuracy per TechInsights

Growth Expected to Favor Besi's Product Portfolio, Particularly Die Attach

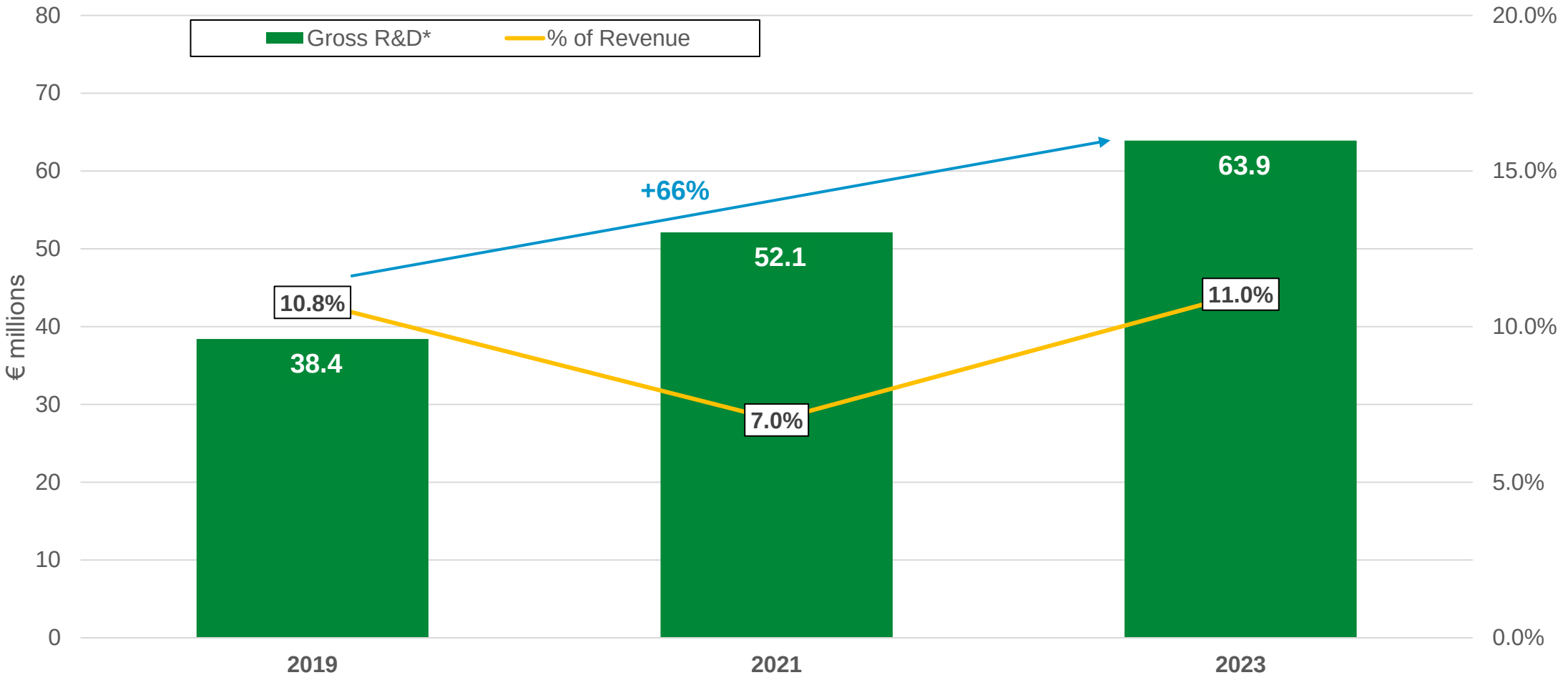
CAGR (2023-2026)	
Die Attach	**29.2%**
Packaging & Plating*	21.8%
Other Assembly	18.5%
Total	**21.6%**



Source: TechInsights, June 2024

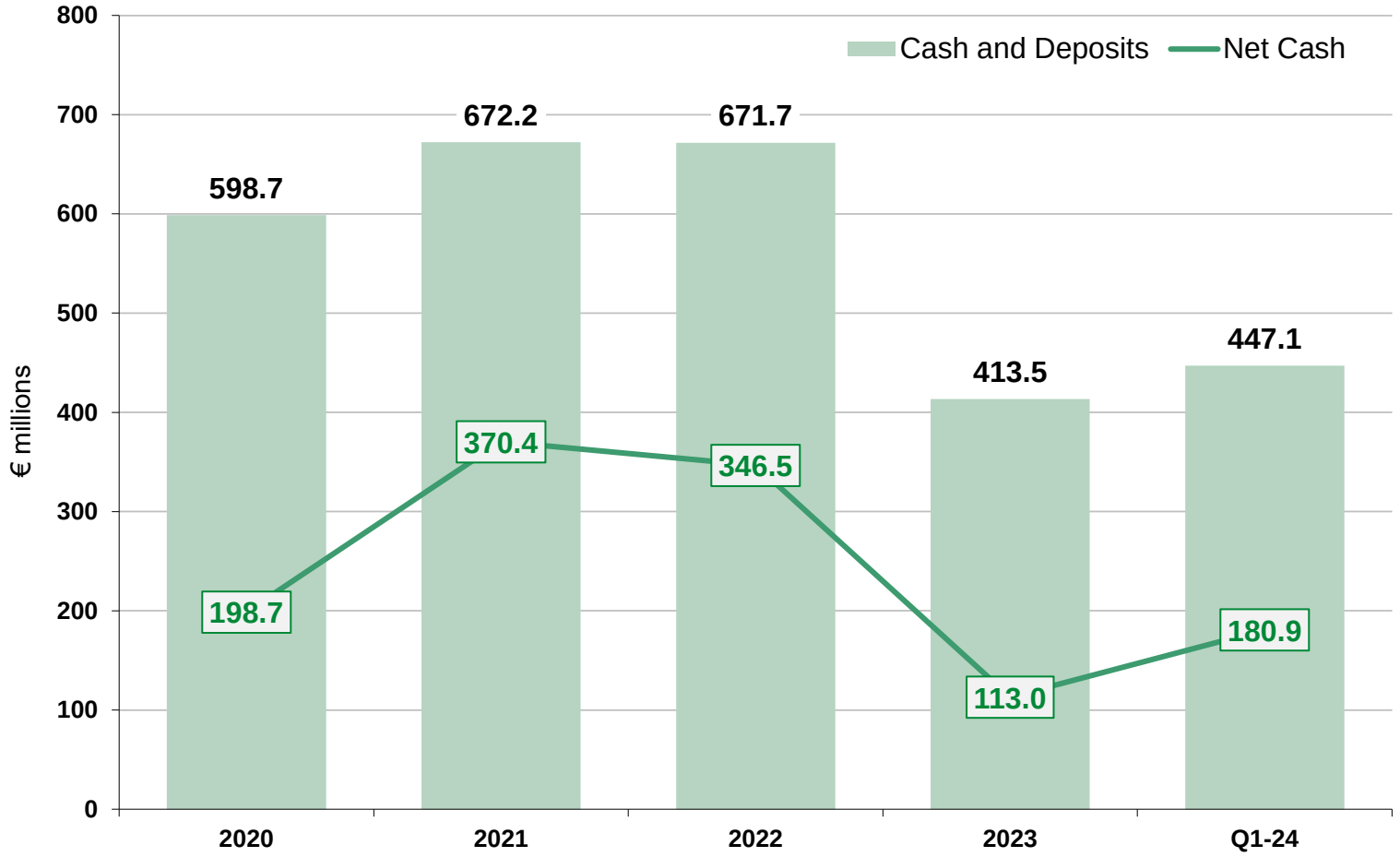
* Packaging & Plating includes only Besi's addressable segments. Non-addressable reported in other assembly market.

Increasing R&D Investment to Capture Next Gen AI Opportunities



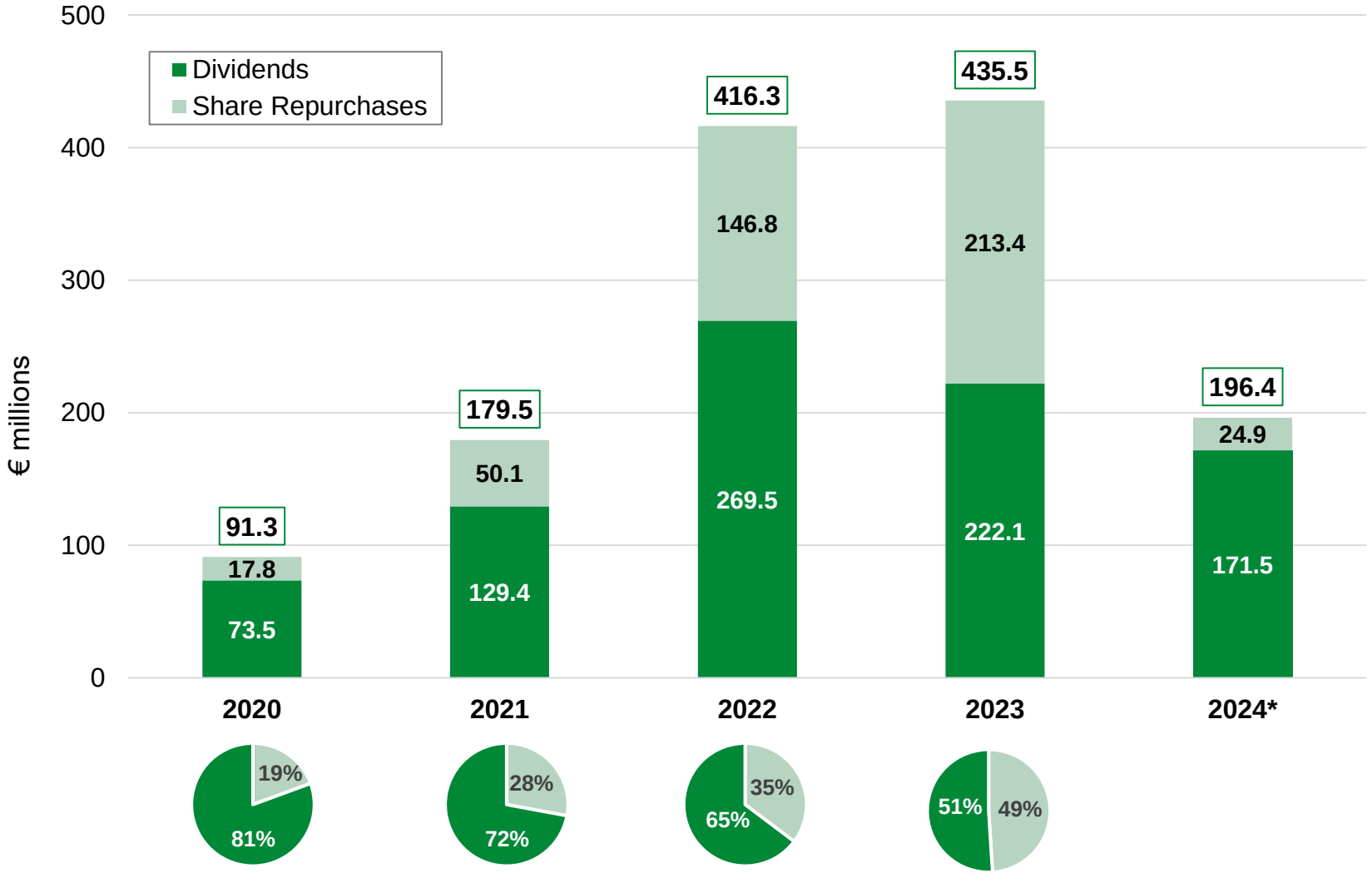
* Gross R&D spending excludes impact from capitalization/amortization of R&D costs.

Strong Liquidity Position Maintained to Finance Future Growth



- **Liquidity position increasing post record 2023 capital allocation**
- **Attractive funding to help finance growth:**
  - **Convertible debt:**
    - Per April 25, 2024: € 200.5 million outstanding
      - Blended interest rate 1.73%
  - **€ 80 million revolving credit facility available**
    - Expandable to € 136 million

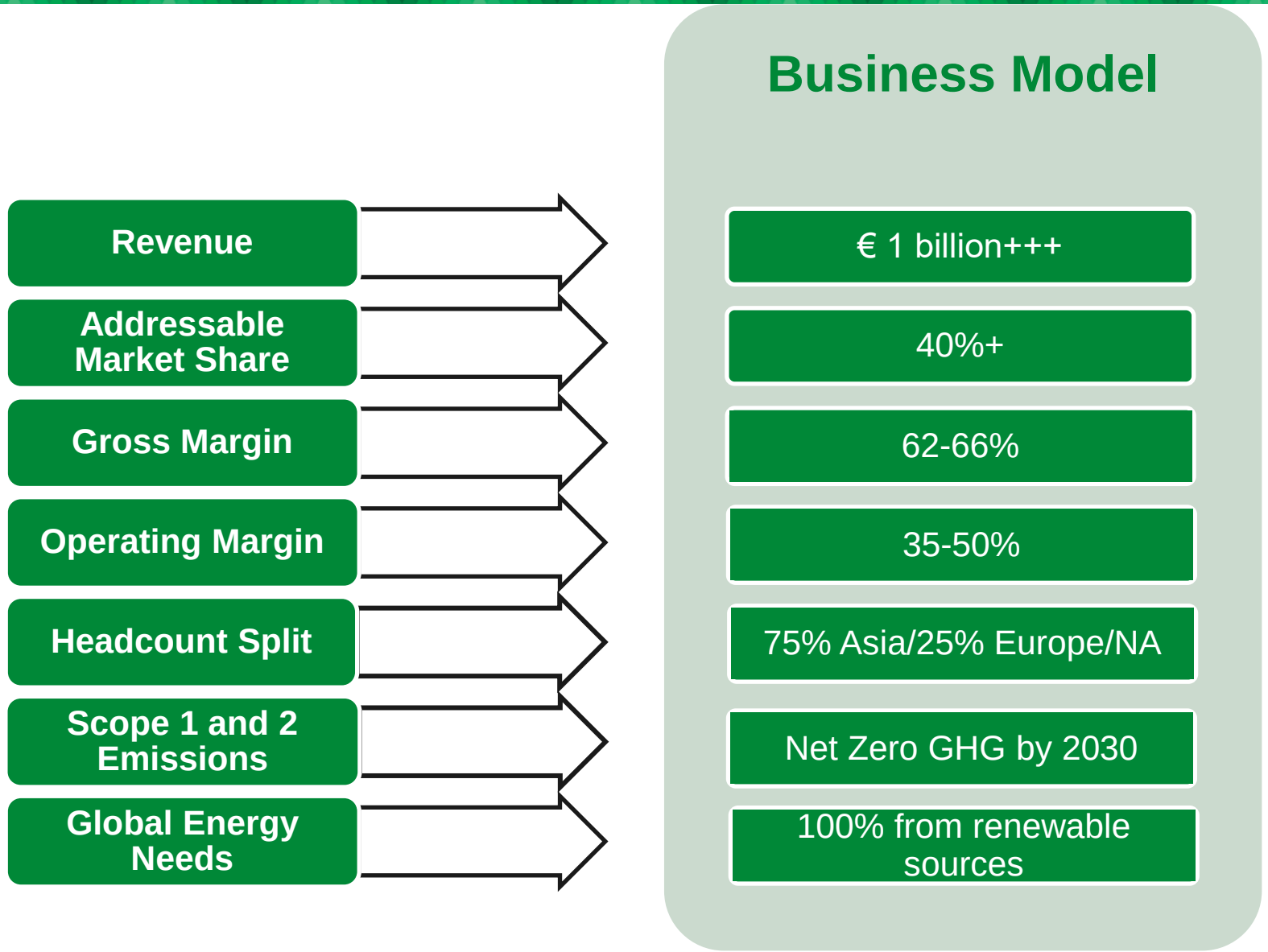
Attractive Capital Allocation Policy Continues



- **€ 2.0 Billion Distributions Since 2011**
  - ~30% of Cumulative Revenue
  - ~€ 196 million distributed in 2024 through May 31
- **€ 34.5 million shares repurchased under current € 60 million authorization:**
  - Avg price of € 136.57

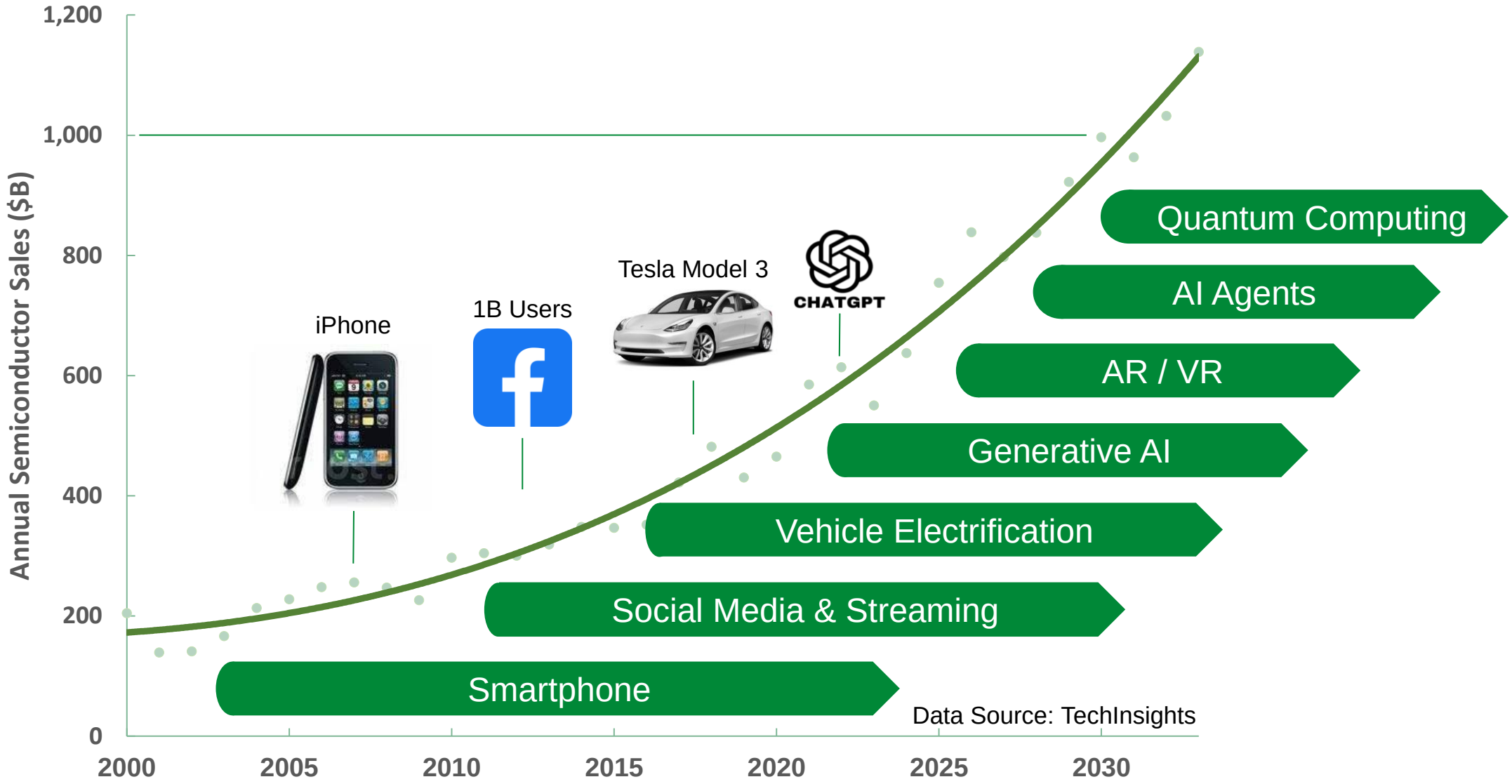
* Includes dividend of € 2.15 per share and share repurchases through May 31, 2024

Business Model



II. MARKET TRENDS
Chris Scanlan
SVP Technology

Semiconductor Sales Expected to Reach $1 Trillion by 2030



AI Driving Growth in Besi's Principal End User Markets

Mobile Internet (30%)	Computing (24%)	Automotive (18%)	Industrial/Other (11%)
 Generated by ImageFX			 Generated by ImageFX
On Device AI	**Generative AI**	**Autonomous Driving**	**Automation**
AR/VR Headsets Camera Technology 5G Advanced → 6G	Datacenter Gaming Si Photonics	Vehicle Electrification Connectivity Infotainment	Smart Grid Industrial IoT Clean Energy

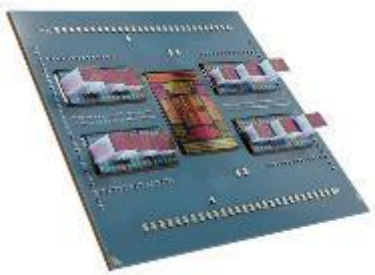
Percentages based on 2023 estimated revenue per end market application. Spares/service revenue was ~17% of 2023 revenue

Particularly for Advanced Logic and Memory Applications

Requiring 2.5D, 3D and chiplet packaging architectures using hybrid bonding, TCB and advanced flip-chip interconnects

Data Center AI Devices

CPU



GPU / Accelerator

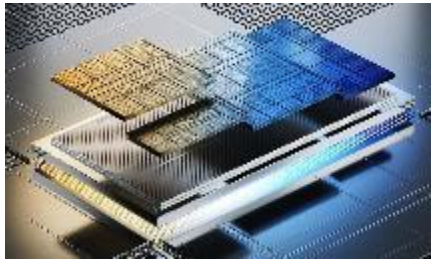
HBM

Sources: AMD, Intel, SK Hynix

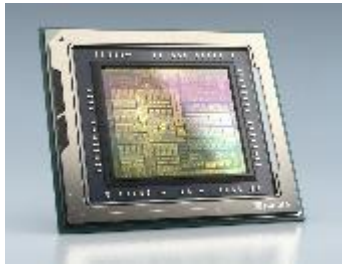
Edge AI Devices

Mobile

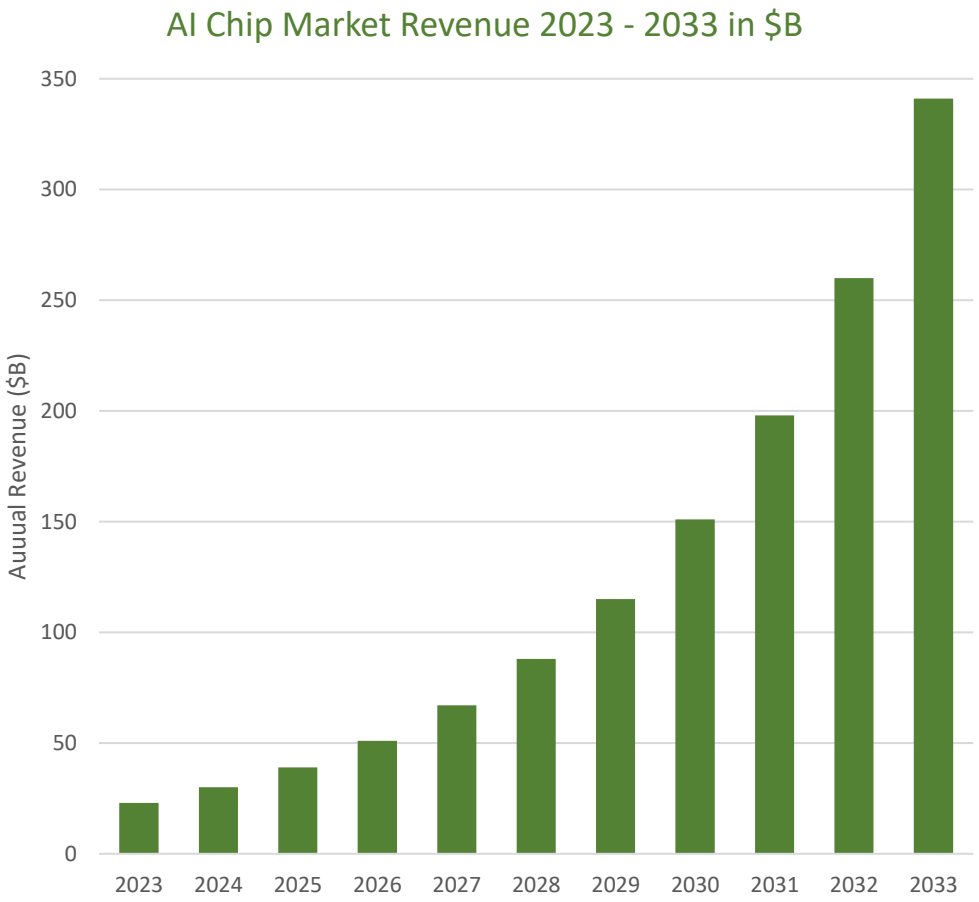
PC



Automotive



Sources: Google, Intel, nVidia

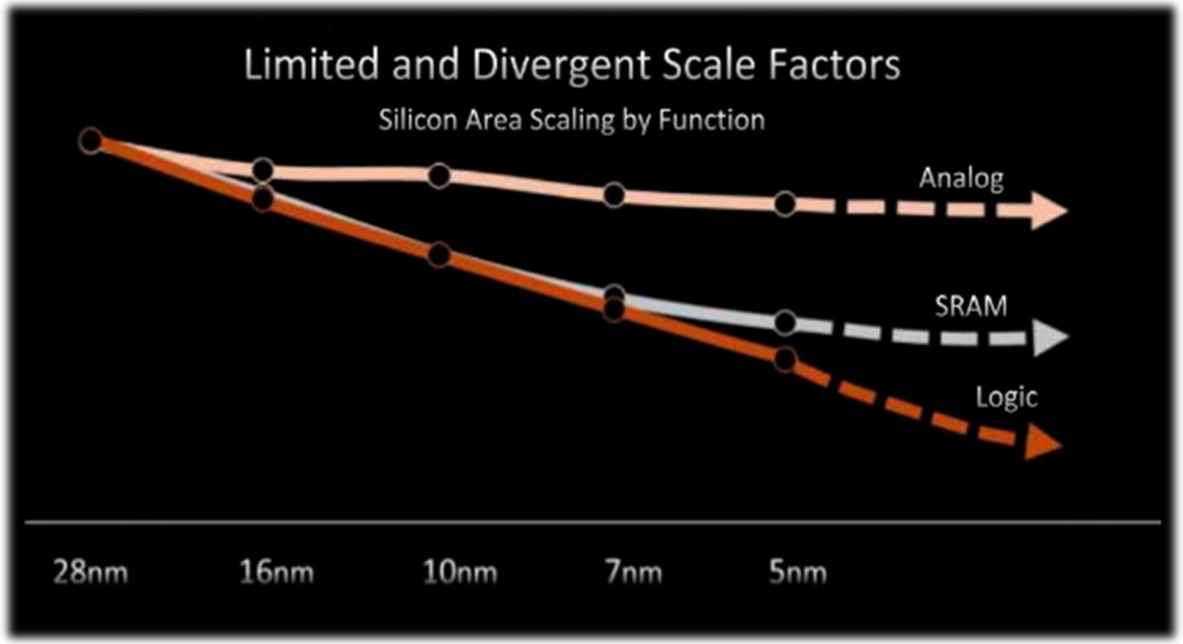


Source: Statistica 2024

Slowing of Moore's Law Drives Adoption of Chiplet Architectures and New Assembly Solutions

Problem

- Moore's Law slowing as data volumes grow exponentially and commercial applications expand
- Cost per transistor increasing
- Die area increasing even as node sizes reduce

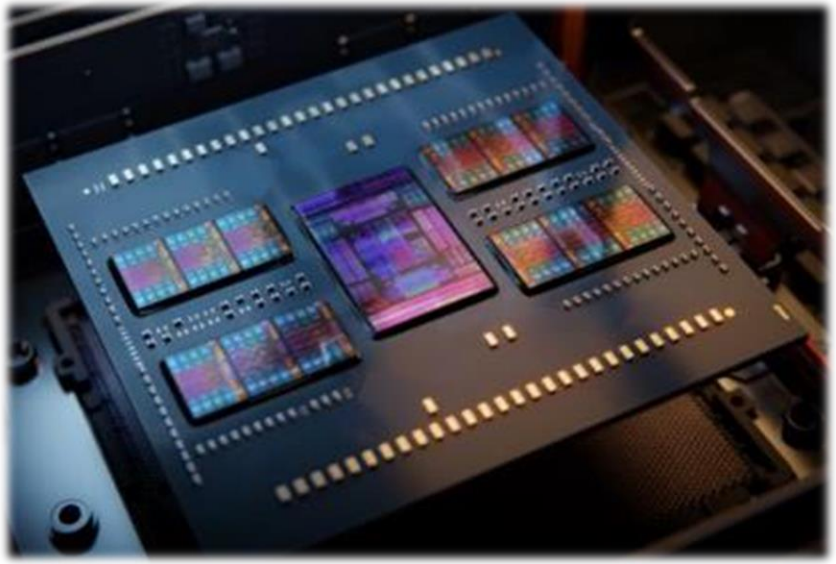


Source: AMD

Solution

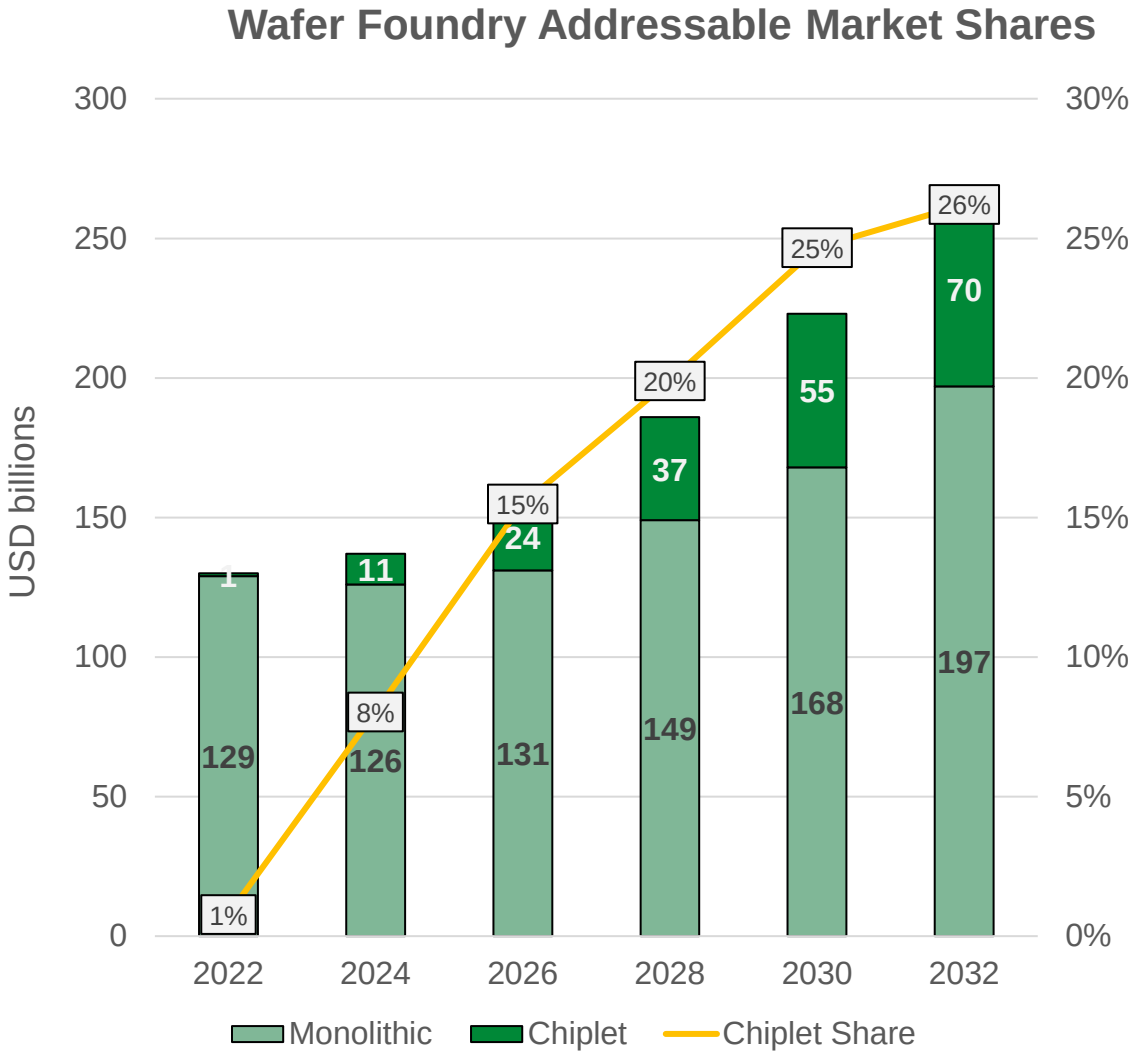
- Split SoC into multiple, smaller **chiplets**
- Optimize scale per function
- Connect chiplets within package utilizing hybrid bonding and C2W TCB

AMD's Genoa X: 25 Active Chiplets in One Package

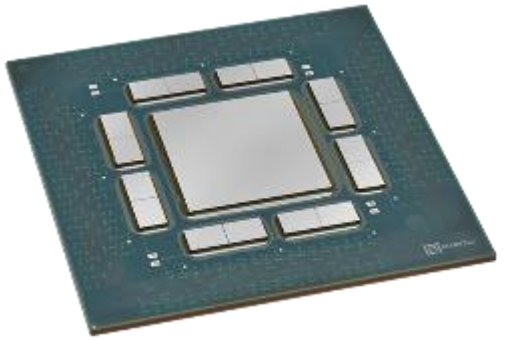


Source: AMD

Chiplet Usage Increasing Rapidly Due to Favorable Economics for Advanced Applications



Source: CSM foundry model, ISM foundry model



Marvell Data Center Switch
17 chiplets

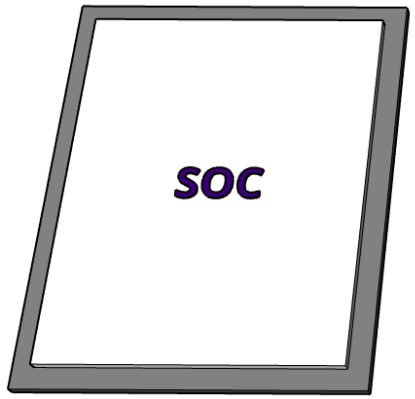
Amazon Data Center CPU
7 active chiplets

Favorable economics due to:

- Reduced die cost
- Increased die yield resulting from smaller die sizes
- Faster development cycle time
- Increased flexibility and technology reuse

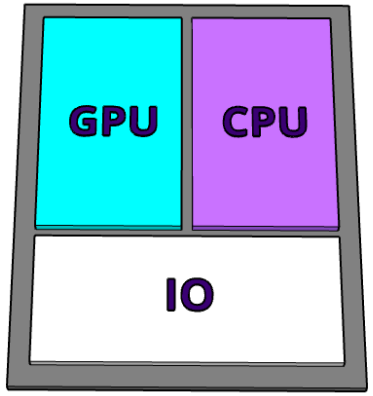
Chiplet Usage Also Drives Higher Capital Intensity

Single Chip Design



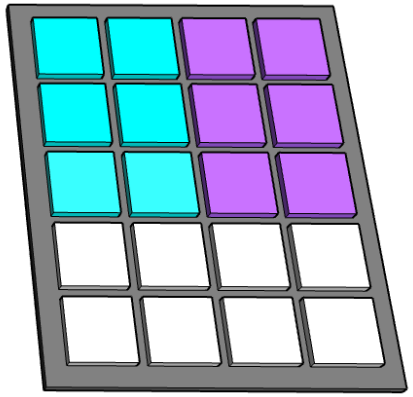
Monolithic: Integrated SoC

Multi Chip Module



Multiple Dies: node optimized

Multi Chiplet System



Individual IPs: node optimized

1 Step	More die attach steps	Dozens
10µm	Higher accuracy	100nm

Source: Intel

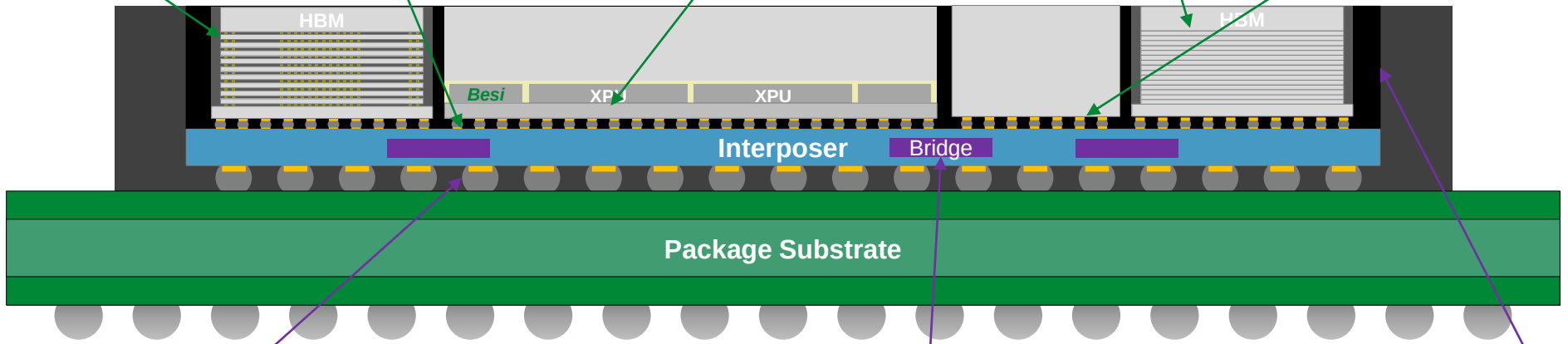
AI Chiplet Packages Use a Variety of 2.5D/3D Assembly Processes

Besi

TCB Chip-to-Wafer	
HBM Die Stacking ≤ 16 memory die	Die to Interposer 10 to 36 µm pitch

Hybrid Bonding	
3D IC Chiplet Stacking ≤ 9 µm pitch	HBM Die Stacking ≥ 16 memory die

Flip-chip C2W
Die to Interposer > 36 µm pitch Mass reflow



Interposer Attach (oS)	
Flip-chip MR Smaller interposers Lower warpage	TCB C2Substrate Larger interposers Higher warpage

Embedded Bridge Attach	
2D Face-up bridge Wafer or panel <1 µm accuracy	3D Bridge w/TSVs Wafer or panel TCB C2W

Molding
Wafer Level MUF Film assisted MUF for interposer encapsulation

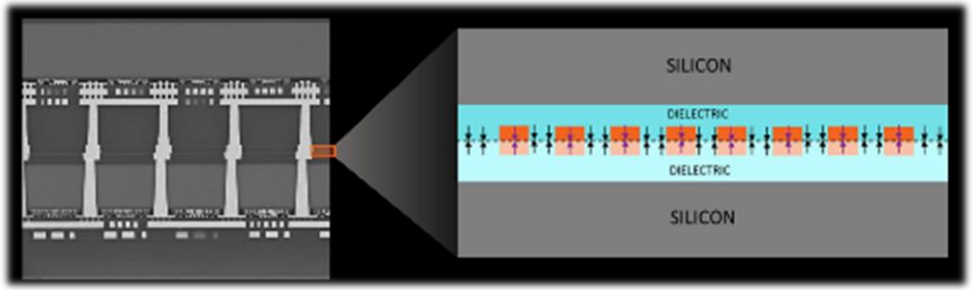
Hybrid Bonding is Technology of Choice for High Performance 3D Chiplet Stacking

Highest performance interconnect to create 3D ICs in front-end wafer fabrication process

TCB C2W used for lower density, less performance critical applications, such as CoW interposer assembly

Hybrid Bonding

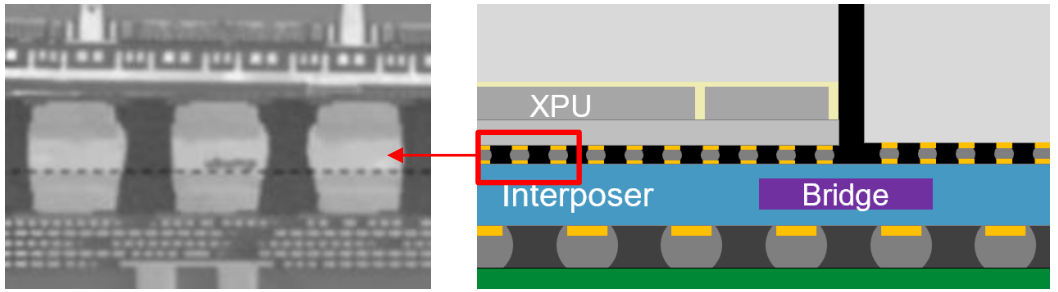
Front-end wafer fab process. Additional steps and features can be added after hybrid bonding to create a 3D wafer.



Source: AMD

TCB Micro-bump C2W

Back-end process. TCB materials are not compatible with front-end fab processes like oxide deposition.



Source: AMD (MI300)

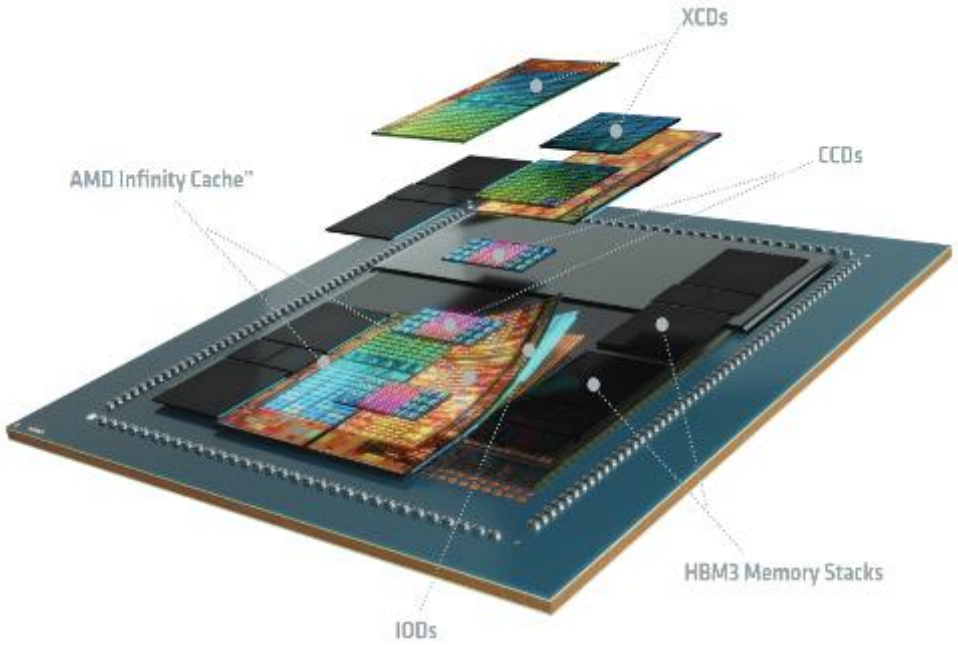
Hybrid Bonding	Performance Factor	Micro-bump C2W TCB
15X	Interconnect Density	1X
11.9X	Speed	1X
191X	Bandwidth Density	1X
1X	Energy / bit	20X

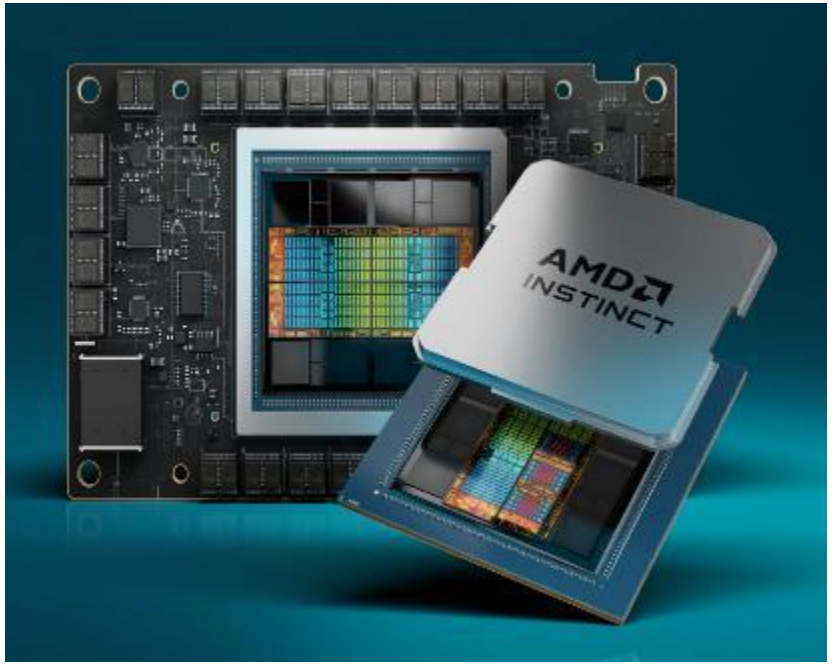
Data source: TSMC

MI300 Illustrates Hybrid Bonding Potential

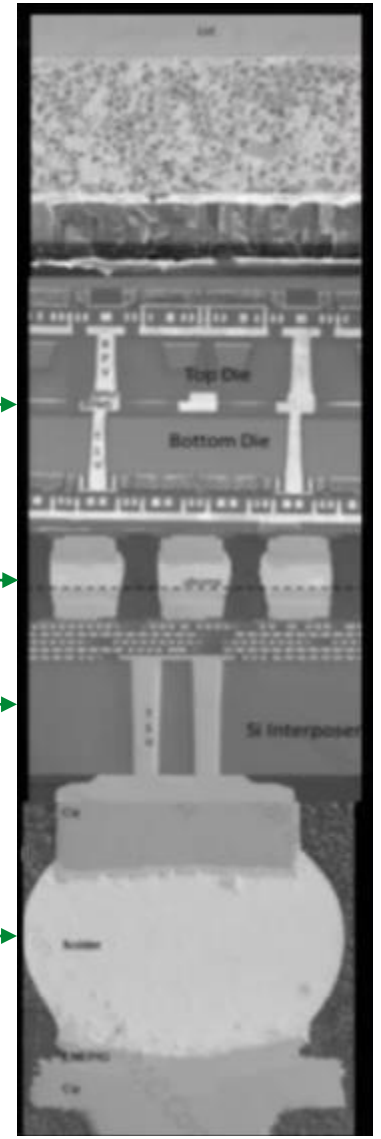
AMD announced 2 versions of the MI300 GPU accelerator device in Dec 2023

- Utilizes hybrid bonding to attach GPU and CPU chips (and spacer die) to a logic base chip
- Assembled base tiles then attached to a TSMC CoWoS-S package using TCB C2W
- Fastest product to reach $1 billion sales in AMD history





Source: AMD

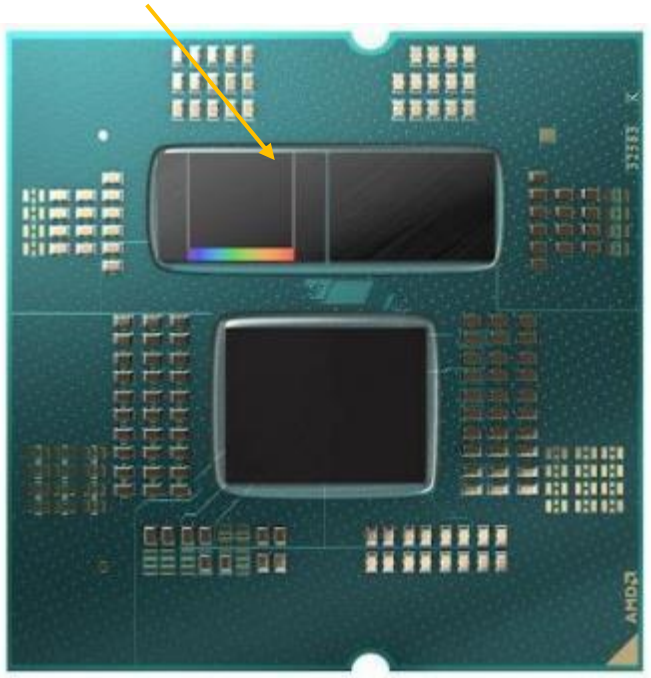


AMD Using Hybrid Bonding for Multiple Product Families In High Volume Production Past Two Years

Ryzen™ 9 7900X3D

- **Gaming processor**
- Hybrid bonding of two Ryzen CCD chiplets + custom I/O chiplet

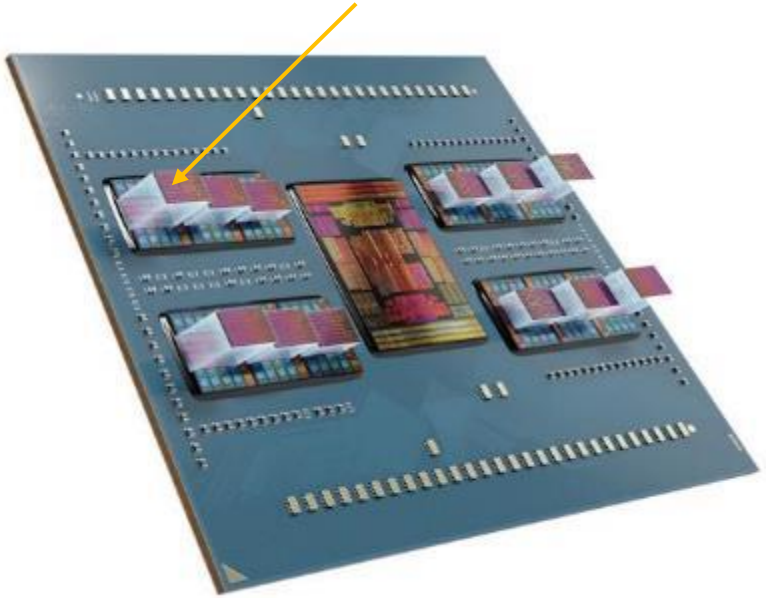
Hybrid bonded CCD chiplet



EPYC™ 9004 Series Processors with 3D V-Cache™

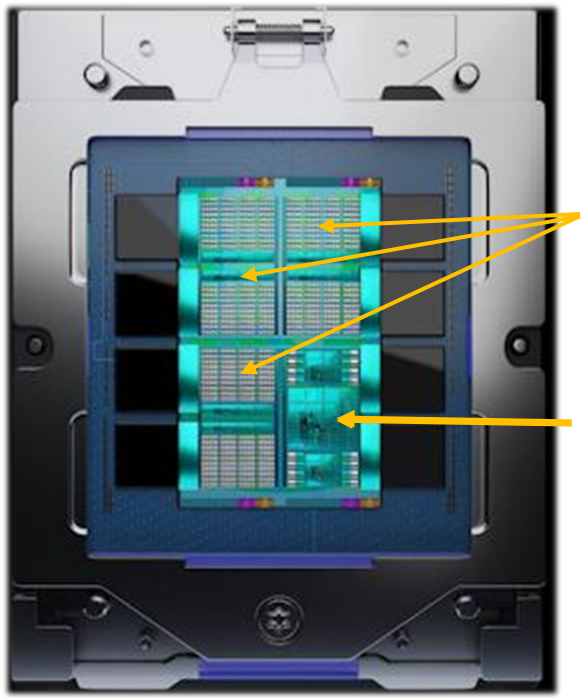
- **Data Center CPU**
- Hybrid bonding of 12 Ryzen CCD chiplets + custom I/O chiplet

Hybrid bonded CCD chiplets



MI300 AI GPU

- **GPU + CPU for super computing**
- First **logic-on-logic** stacking with D2W hybrid bonding



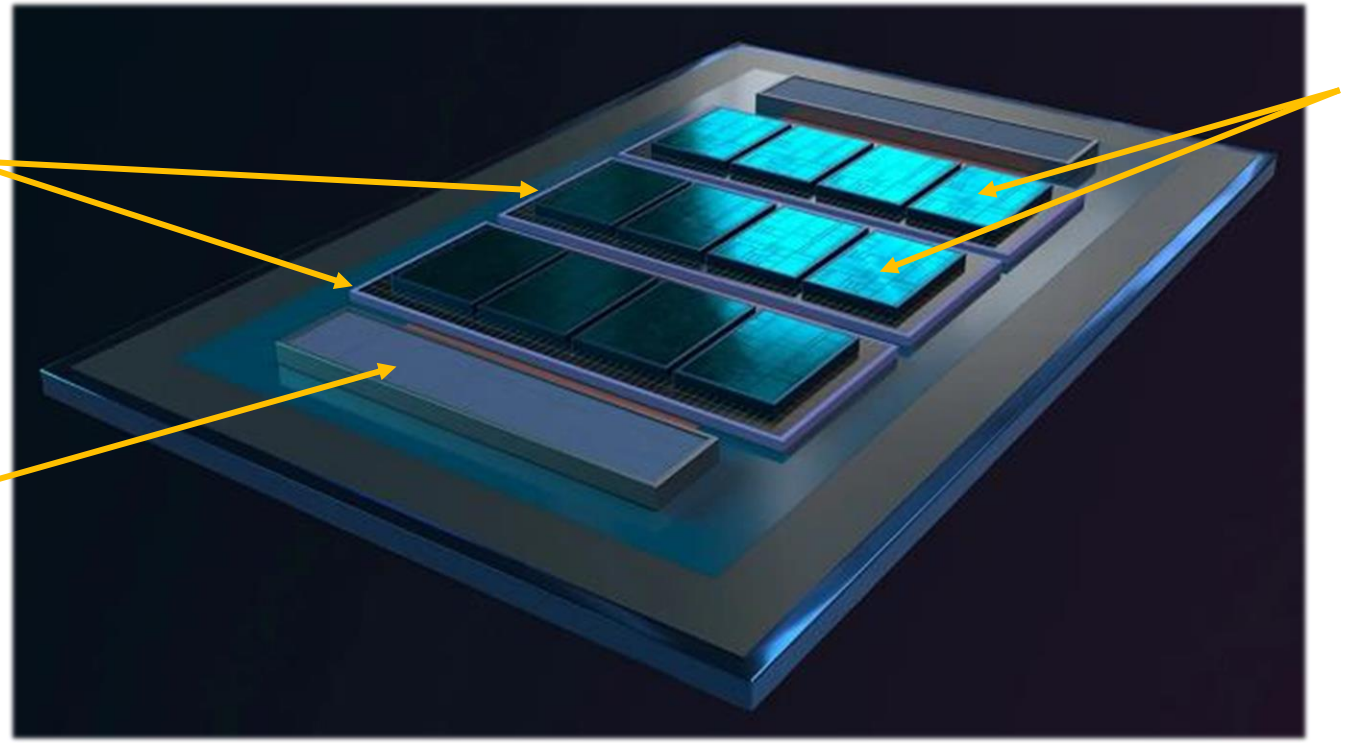
Intel Clearwater Forest CPU is Next Major Hybrid Bonding Launch

- First Intel CPU product using hybrid bonding to stack CPU core chiplets atop base tiles with SRAM and I/O functions
- Attaches up to 12 CPU chiplets to functional base tile
- **3D stacking *"improves the latency between compute and memory by shortening the hops, while at the same time enabling a larger cache"* - Pushkar Ranade, Intel**

3 I/O chiplets with main SRAM, voltag regulators and internal network function

Fabricated on Intel 3 nm node

I/O system on two dies built using Intel 7



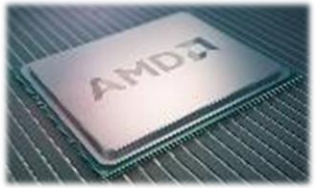
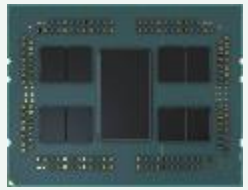
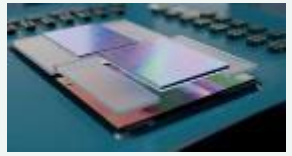
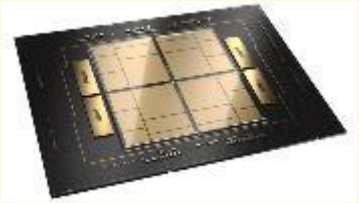
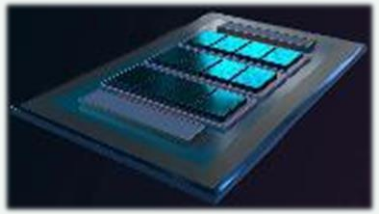
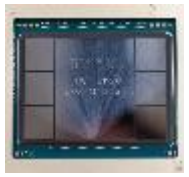
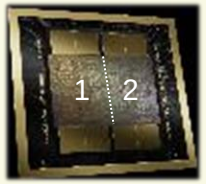
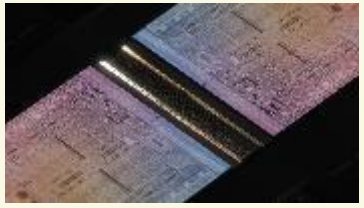
12 CPU chiplets fabricated on Intel 18A node

3D stacking of CPU chiplets to base die using **hybrid bonding**

Total 300 billion transistors

Source: Intel

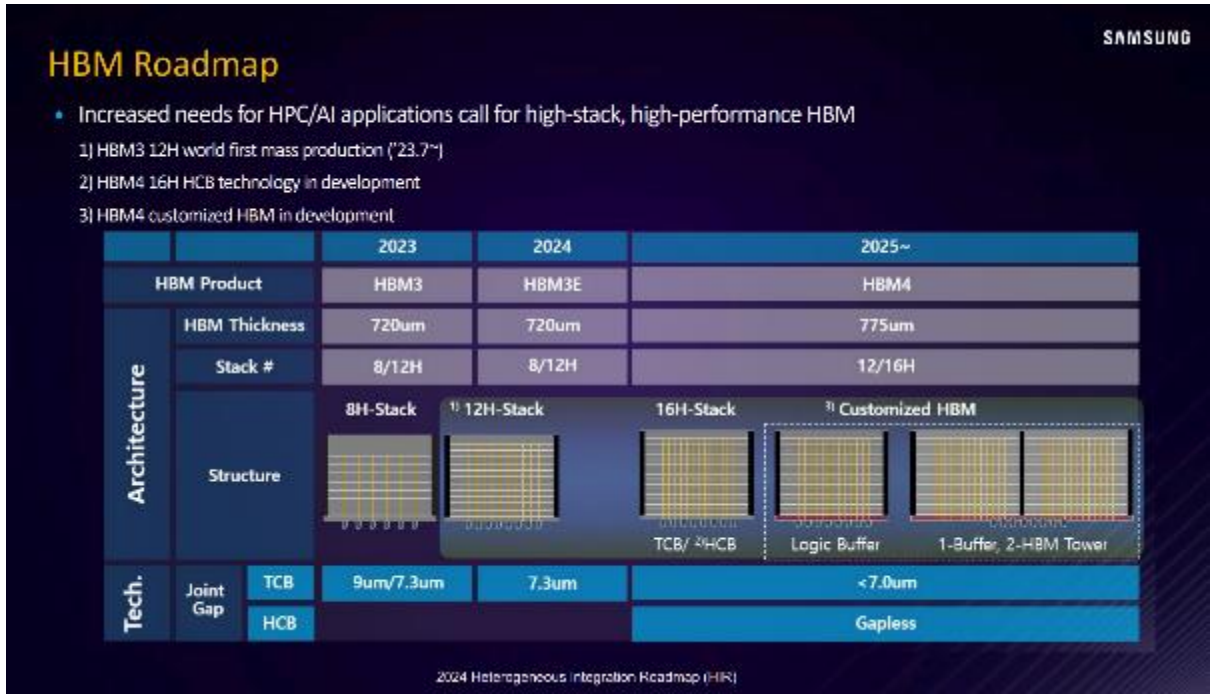
High Performance Processor Evolution

	SoC	Split Die	Chiplets and Hybrid Bonding	
AMD	Opteron Server CPUs 	1st Gen EPYC CPU (2017) 	2nd Gen EPYC (2019) 	3rd Gen EPYC (2022) with Hybrid Bonding 
intel	3rd Gen Xeon CPU 	Sapphire Rapids CPU (2023) 	Clearwater Forest CPU w/ Hybrid Bonding (2025) 	
NVIDIA	H100 GPU 	B100 GPU (2024) 		
Apple	M1 Max CPU 	M1 Ultra CPU (2022) 		

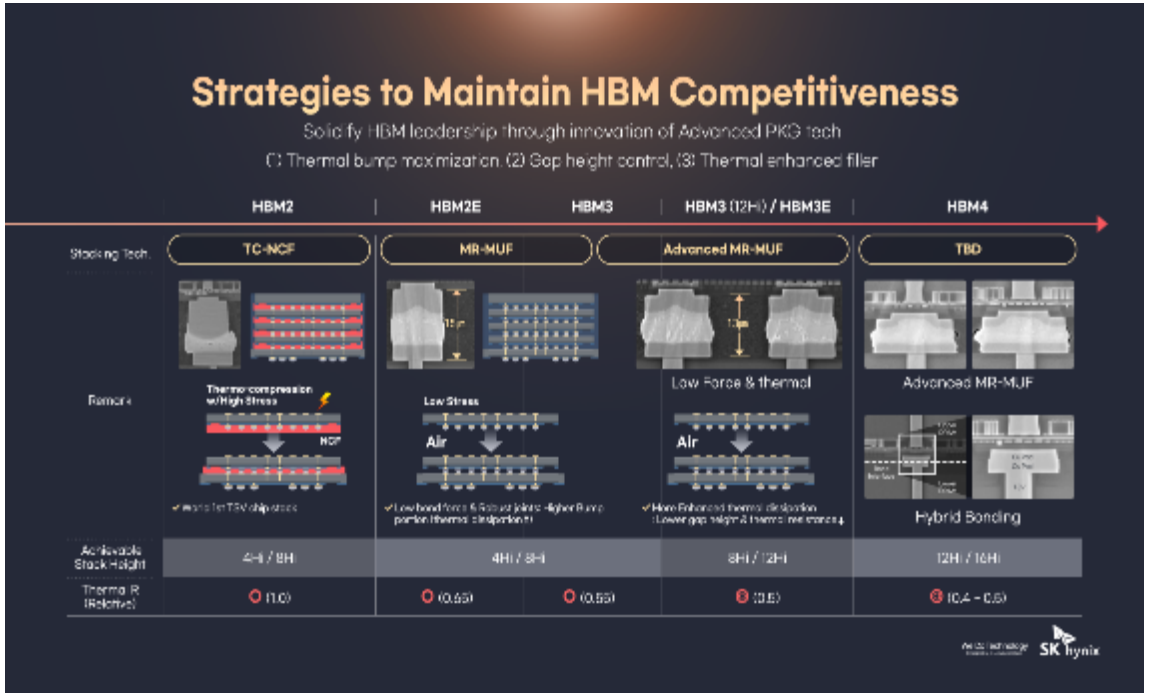
Future chiplet architectures

Hybrid Bonding and TCB on Roadmaps of All HBM Suppliers

- **JEDEC increased the maximum thickness of HBM4 recently to permit stacking of up to 16 die using TCB**
- **Some hybrid bonding adoption expected in HBM4 for higher performance applications in preparation for HBM 5**
- **HBM5 with up to 20 die stack can only be produced using hybrid bonding**
- Samsung and SK Hynix developing both hybrid bonding and TCB micro-bump in parallel for HBM4
- TSMC has developed base logic die for HBM4 on its N5 node optimized for hybrid bonding



Source: Samsung



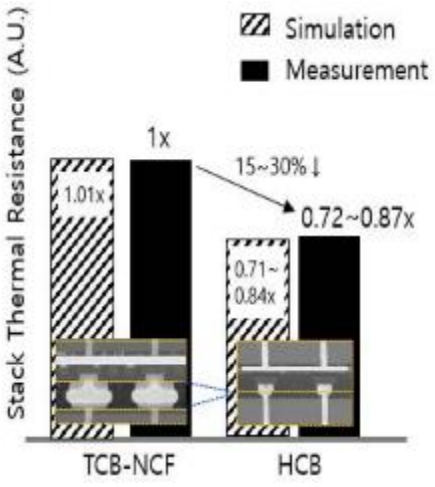
Source: SK Hynix

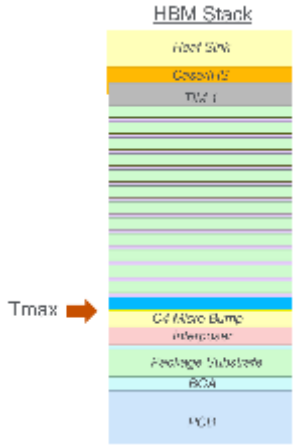
Hybrid Bonding Significantly Improves HBM Performance

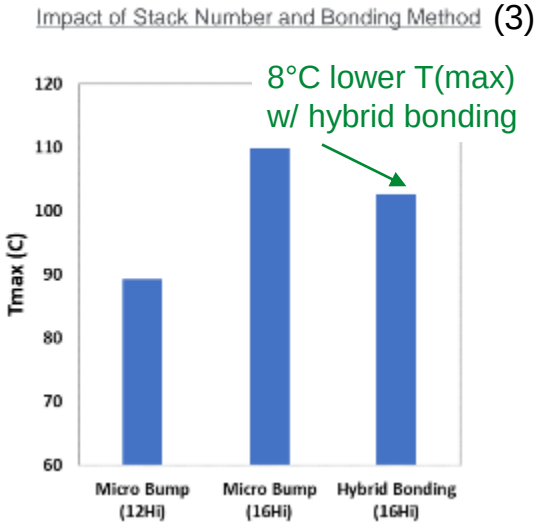
Hybrid bonding outperforms TCB/micro-bump for HBM stacking:

- 20% lower stack thermal resistance [1]
- 20% improvement in signal integrity [2]
- 17% reduction in dynamic power consumption [2]
- 87% reduction in TSV interconnect area [2]

"the power, performance, and area (PPA) metrics of both stacking techniques are analyzed and compared. In all aspects, the hybrid bonding technique is more effective." [2]

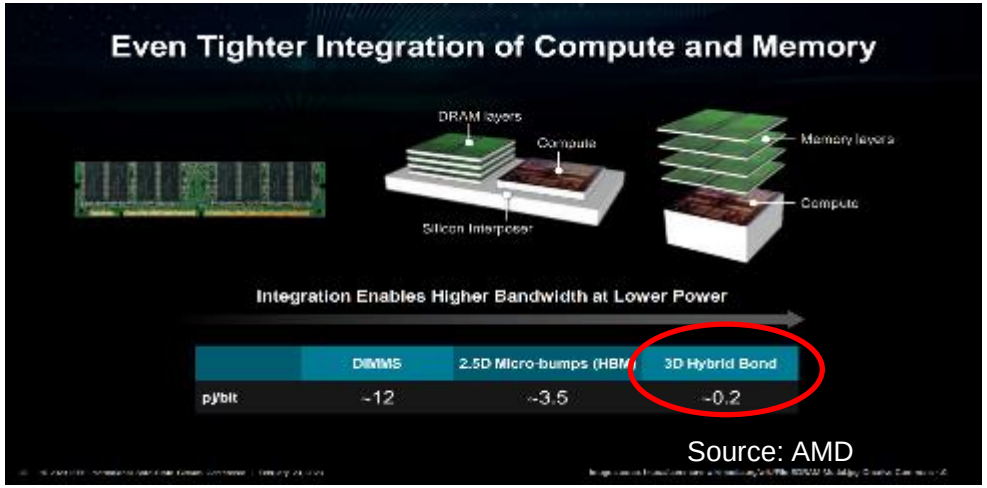


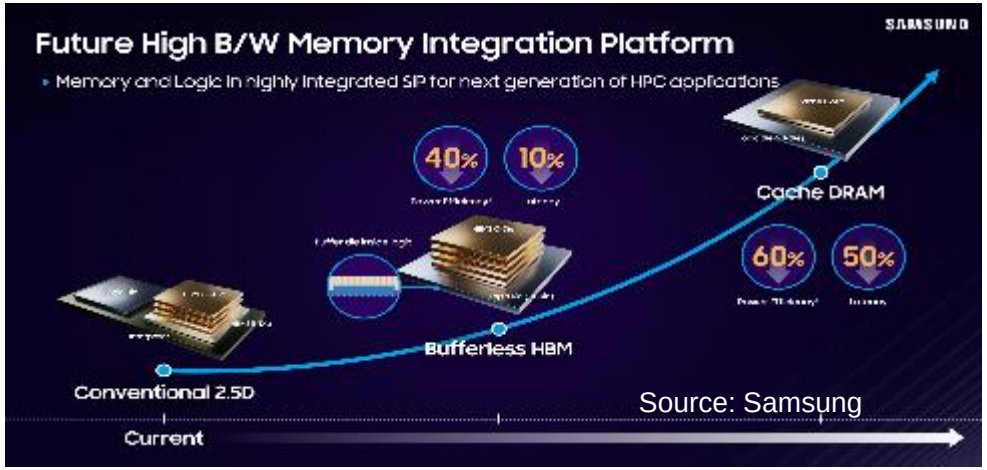




1) "Thermal Improvement of HBM with Joint Thermal Resistance Reduction for Scaling 12 Stacks and Beyond", **Samsung**, 2023
2) "HBM3 PPA Performance Evaluation by TSV Model with Micro-Bump and Hybrid Bonding", 2023 IEEE EPEPS
3) "D2W Hybrid Bonding Challenges for HBM", Applied Materials & Besi, International Memory Workshop 2024

Future direct stacking of DRAM onto logic using hybrid bonding for highest performance





GPU and AI Accelerator Devices Driving 2.5D Package Growth

CoWoS = (Chip-on-Wafer-on-Substrate)

Chip-on-Wafer (CoW)

- Flip-chip attach of logic and HBM to the interposer wafer

On Substrate (oS)

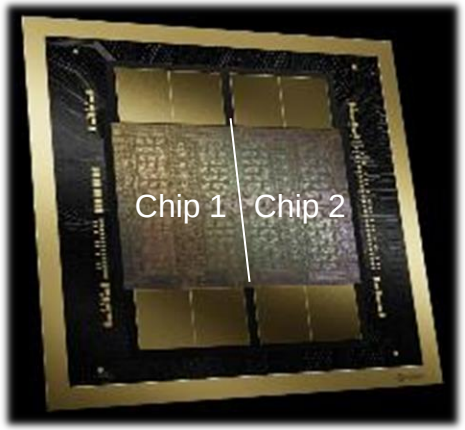
- Flip-chip of interposer module to substrate

Besi equipment used for multiple process steps

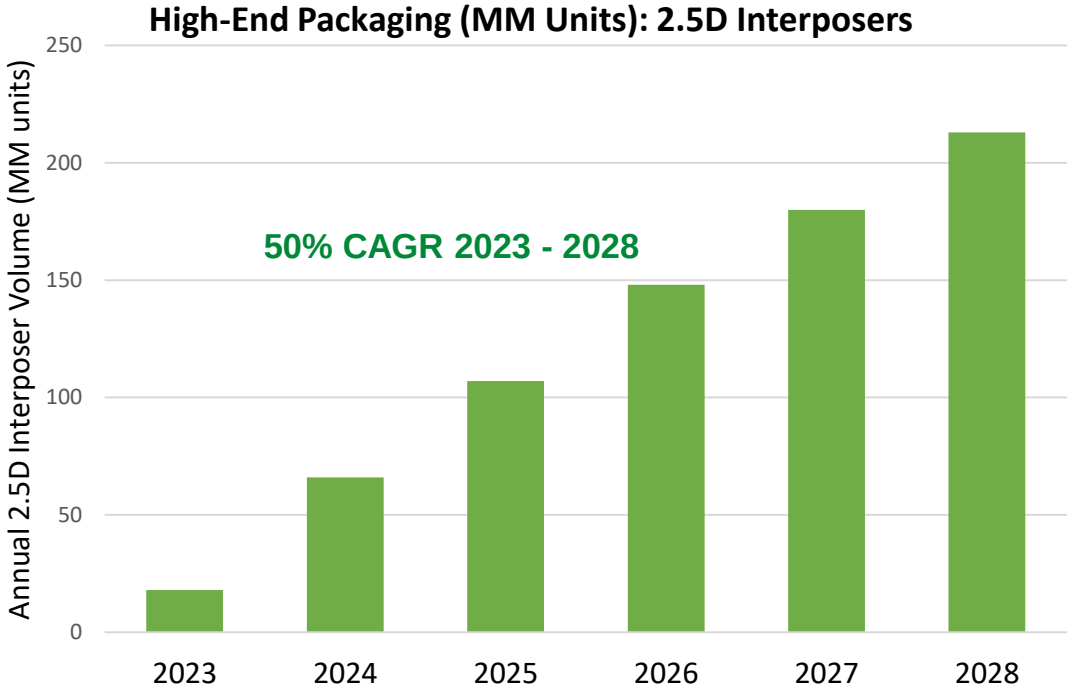
AWS Trainium 2 AI Accelerator

Source: AWS

nVidia B100 GPU



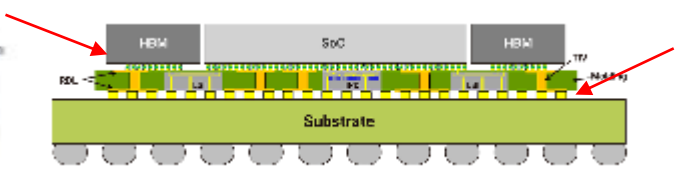
Source: Nvidia



Source: Yole 2024

8800 Chameo

CoWoS-L



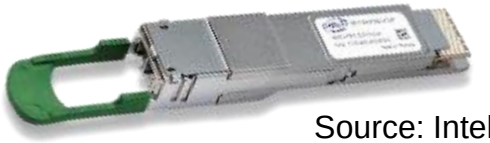
Source: TSMC

2200 evo

AI Servers Driving Growth of Optical Transceivers
Adoption of Hybrid Bonding for Photonic Chiplets Anticipated

Pluggable Optical Transceivers

- Transceiver market growth increasingly driven by AI server clusters
- Besi equipment is used to assembly multiple components



Source: Intel

2200 EVO Advanced

Laser and PIC attach

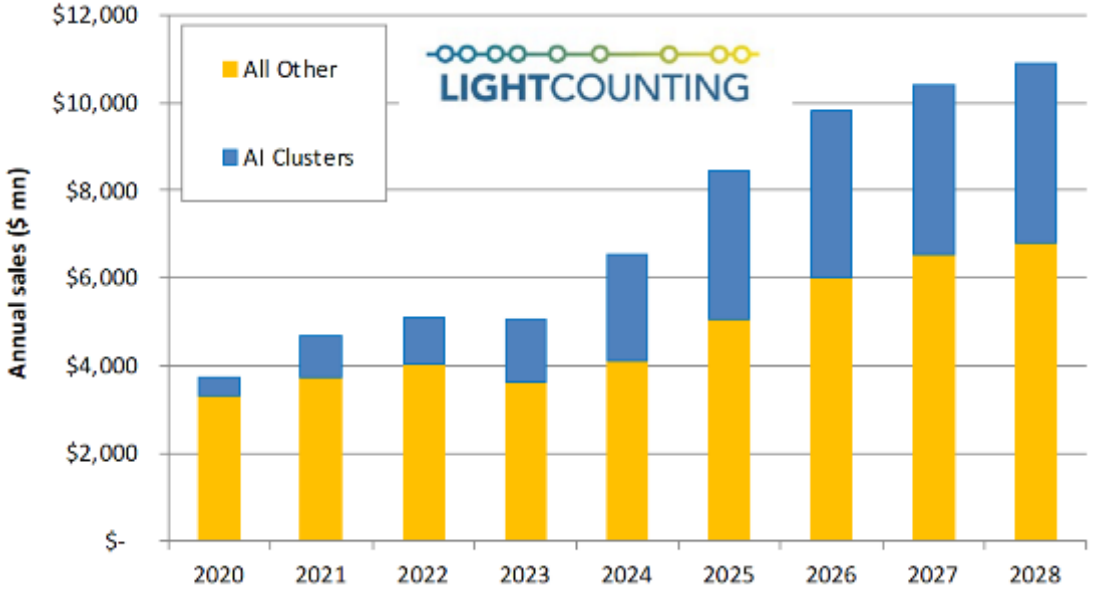
Co-Packaged Optics

- TSMC's COUPE photonic engine technology using hybrid bonding (SoIC-X)
- Qualification of pluggable transceivers planned for 2025. Co-packaged optics by 2026*

https://pr.tsmc.com/english/news/3136

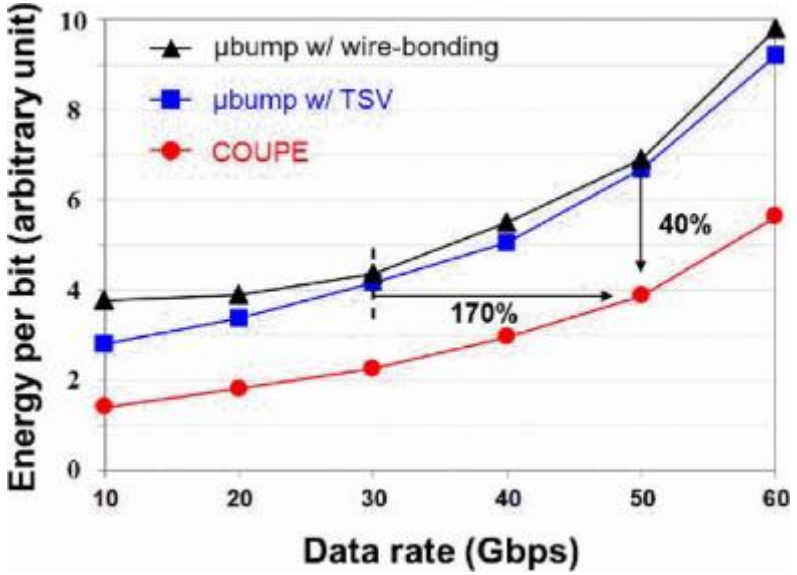
Hybrid Bonder

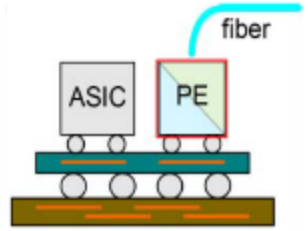
Sales of Ethernet Optical Transceivers By Application



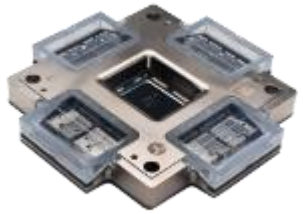
Source: Lightcounting, July 2023

COUPE w/ Hybrid Bonding: 40% lower energy per bit vs. µbump





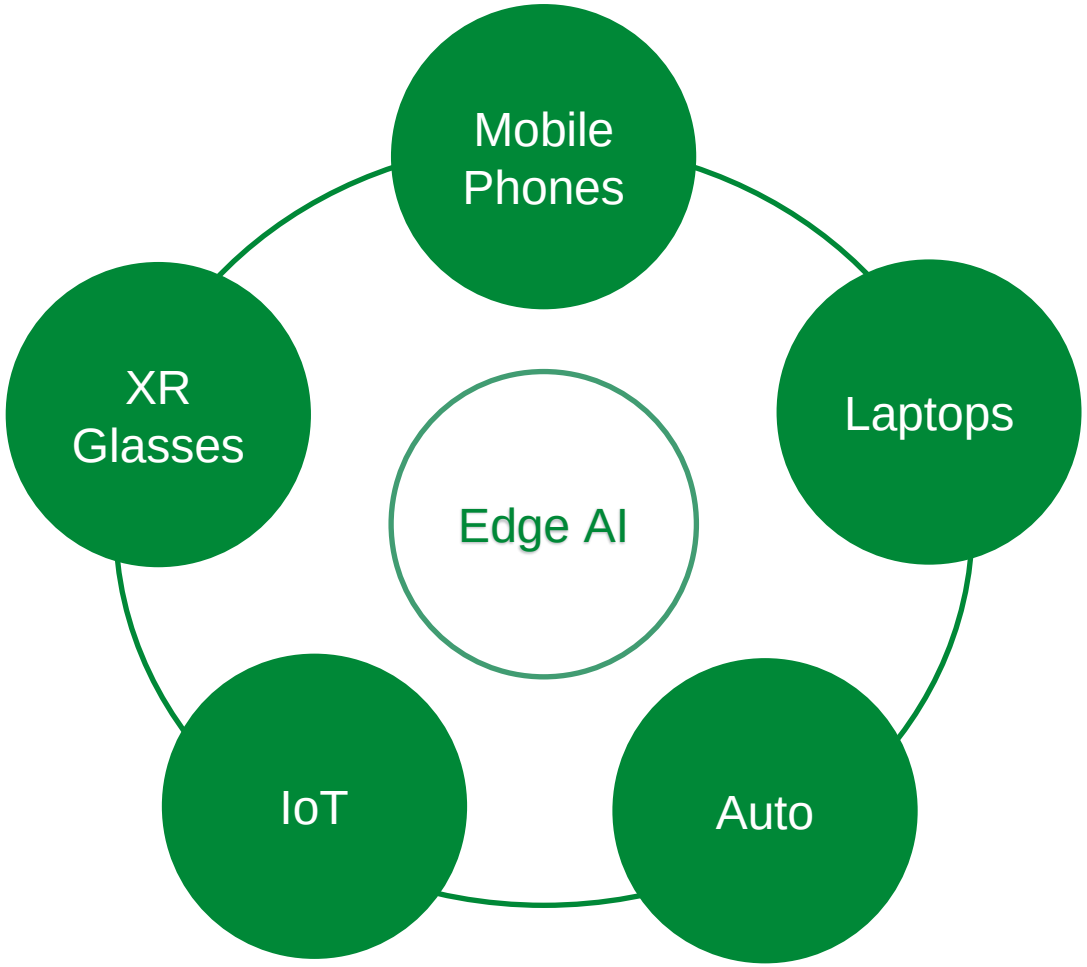
(C) Co-Packaged Optics



Source: Broadcom

Source: TSMC @2021 ECTC

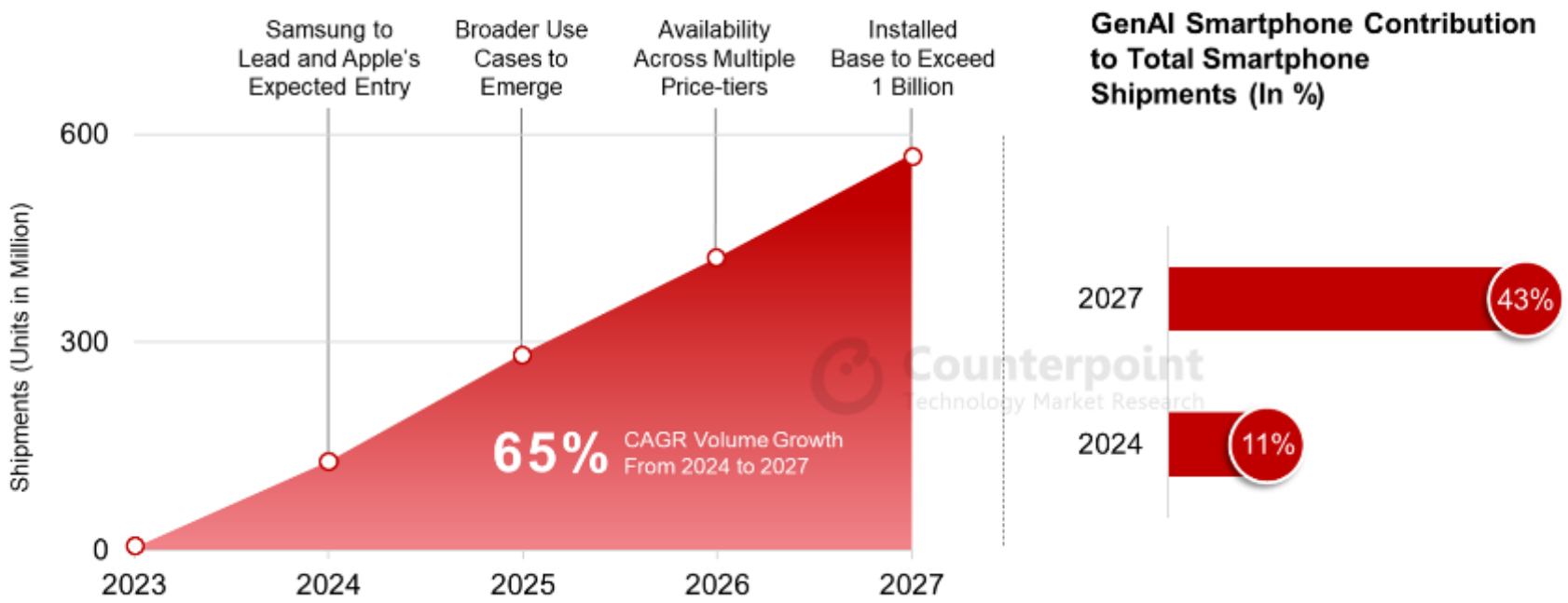
Edge AI Computing Drives Next Generation Consumer Applications

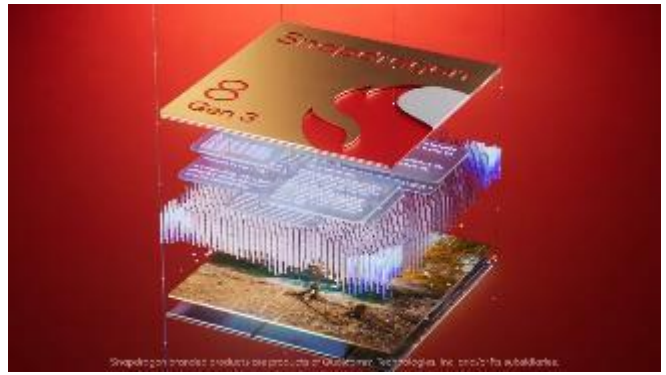


- Edge AI Use Cases
- Text Generation
- Audio and Video Creation
- Image and Video Enhancement
- Code Generation
- Medical Diagnostics
- Auto Self-Driving
- Environmental Monitoring

AI Enabled Smartphones Expected to Drive Smartphone Upgrade Cycle

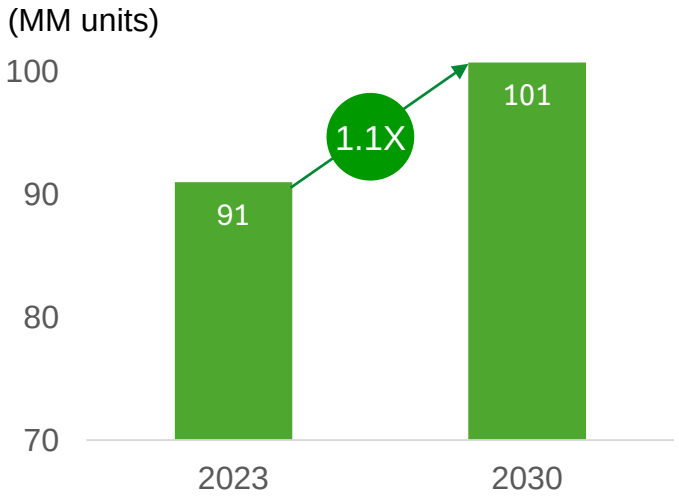
- **Next-gen AI smartphones use processors capable of running on-device GenAI models more quickly and efficiently**
- **Expected transition of APU/NPU from SoC to Chiplet architectures**





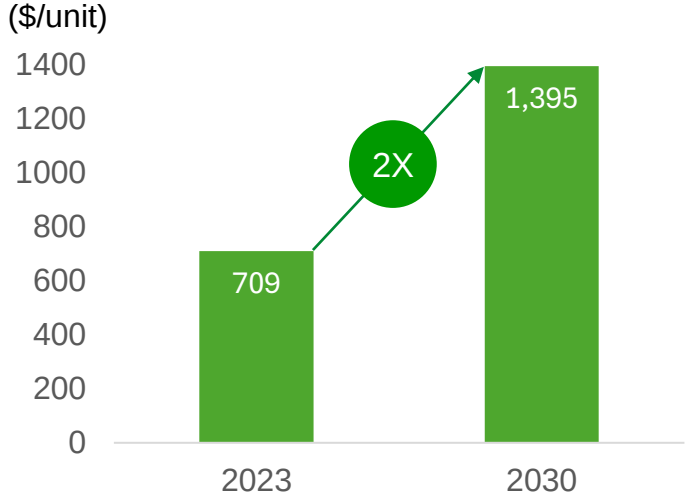
Favorable Long-Term Automotive Semiconductor Outlook Will Aid Each of Besi's Product Groups

Global Vehicle Production



X

Avg. Semiconductor Content Per Vehicle*



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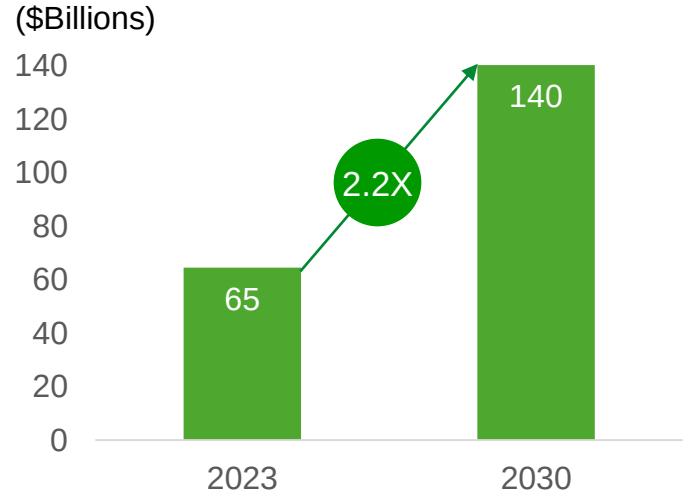
Automotive Semicondcutor TAM*

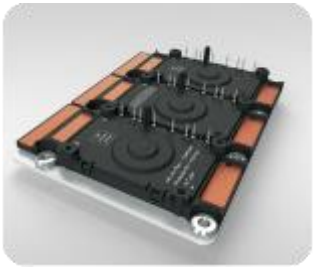


Source: TechInsights

*excluding sensors

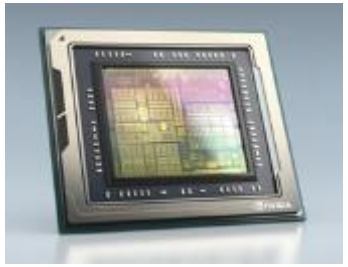
EV Drive Train

Source: Infineon



Source: Semikron Danfoss

AI Self-Driving



Source: nVidia

MCU

Source: ST Micro

Communication

Source: Qualcomm

ADAS

Source: NXP

III. Wafer Level Assembly
Peter Wiedner
Senior VP Sub-Micron Die Attach

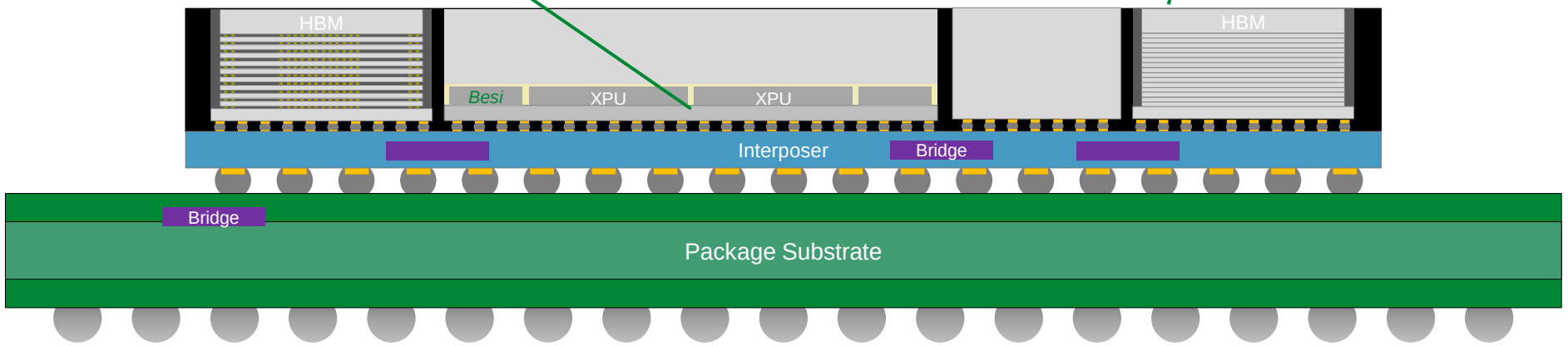
AI Adoption Driving HBM & HPC

High Power Computing

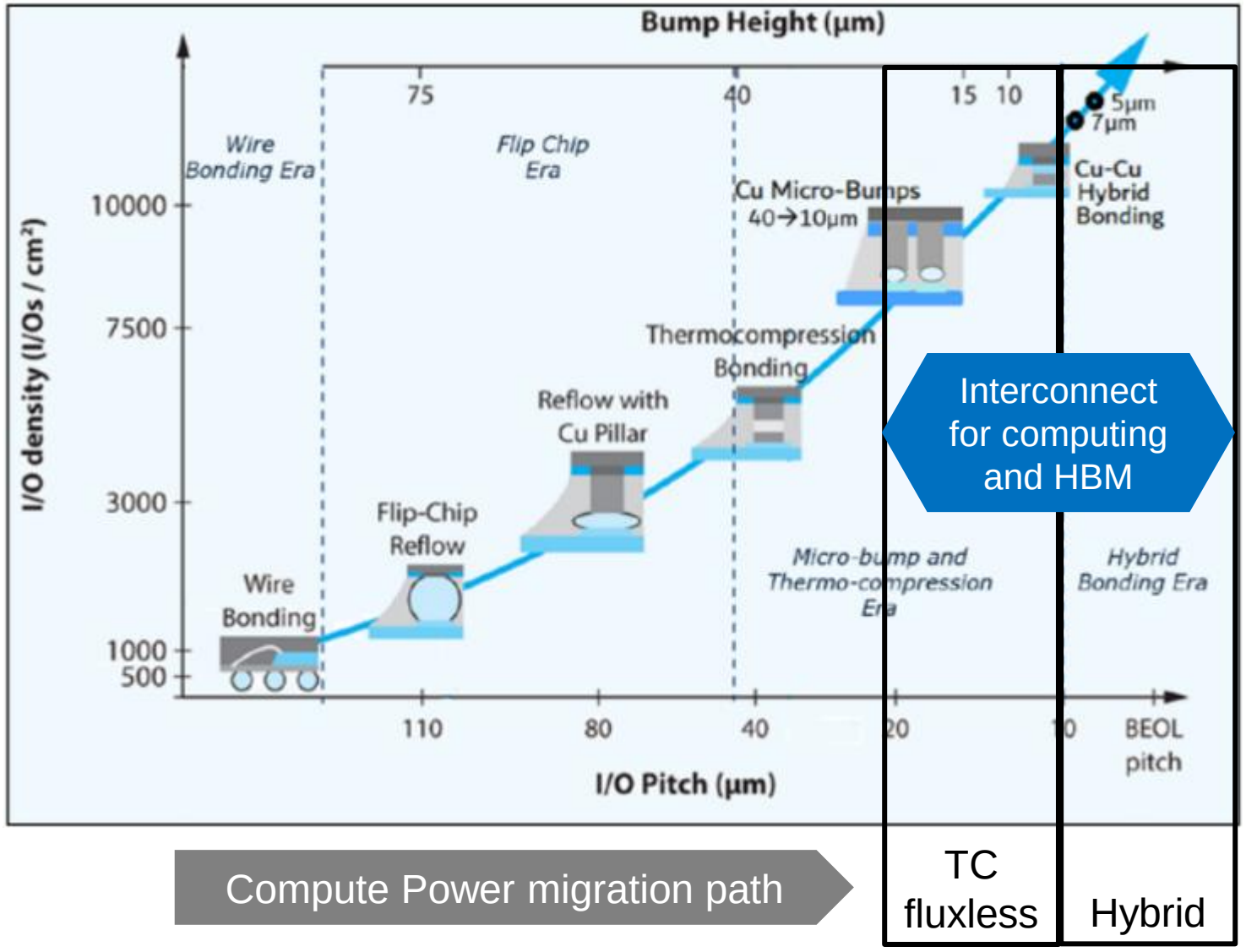
Hybrid dominant interconnect technology for HPC

High Bandwith Memory

Hybrid and TCB complementary technologies – Both needed for next gen HPC



Advanced Logic Driving New Fine Pitch Interconnect Technologies



- High end semiconductors always follow path to smallest bump pitch
- Hybrid enables bump pitches <10µm Facilitates 3D chip designs to extend Moore's law
- TC fluxless bridges the gap between existing flux-based TCB and Hybrid interconnect

Hybrid Bonding Product Roadmap

Generation 1: 200nm

Industry Standard for Hybrid Bonding

Generation 2: 100nm

New Standard: 100nm Bonder

10% Productivity increase

Generation 3: 50nm

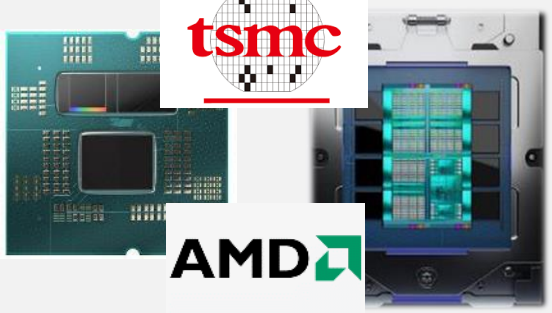
Working on 50nm Bonder

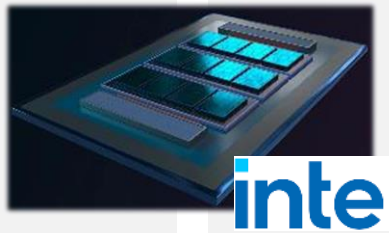
30% Productivity increase

Bump Pitch

10 µm | 9 µm | 8 µm | 7 µm | 6 µm | 5 µm | 4 µm | 3 µm | 2 µm | 1 µm

2023 | 2024 | 2025 | 2026



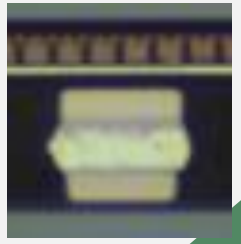


Thermo Compression Product Roadmap

9800 TC Next
1µm

Lowest Cost of Ownership

9800 TC Fluxless
0,5µm



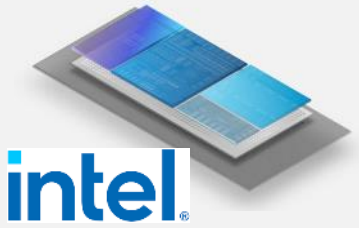
High Accuracy without UPH impact

Integrated Hydroxyl Reduction

Bump Pitch

40 µm | 35 µm | 30 µm | 25 µm | 20 µm | 15 µm | 10 µm

2023 | 2024 | 2025 | 2026



HBM Evolution: Ever Increasing Number of Layers, Capacity and Bandwidth in Each Successive Generation

HBM PRODUCT DEVELOPMENT – OVERVIEW

HBM generation	HBM	HBM2	HBM2E	HBM3	HBM3E / HBM3P[1]	HBM4 / HBMNext[2] (expected)
Players with market products	SK hynix	SAMSUNG, SK hynix Flarebolt Aquabolt Aquabolt-XL (PIM)	SAMSUNG, SK hynix, Micron Flashbolt	SAMSUNG, SK hynix Icebolt	SAMSUNG, SK hynix, Micron Shinebolt	SAMSUNG, SK hynix, Micron
Year of first product release	2014	2018	2020	2022 - 2023	2024	2026
Typical number of dies per stack (Main packaging approach)	4Hi (TSV & microbumps)	4-8Hi (TSV & microbumps)	4-8Hi (TSV & microbumps)	8-12Hi (TSV & microbumps)	8-12Hi[3] (TSV & microbumps)	12-16Hi (Cu-Cu hybrid bonding for 16Hi)
Max capacity per stack	1GB	4-8GB	8-16GB	16-24GB	24-36GB	36-64GB
Die density (Typical process)	2Gb (2x)	8-16Gb (2y, 2z)	16Gb (1y, 1z)[4]	16Gb (1z)	24Gb (1a, 1b/1β)[5]	24-32Gb (1b/1β, 1c/1γ)
Max data rate	1Gbps	2-2.4Gbps	3.2-3.6Gbps	5.6-6.4Gbps	8.0-9.8Gbps	≥ 9Gbps
Effective bus width	1,024	1,024	1,024	1,024	1,024	2,048
Max bandwidth per stack	128GB/s	205-307GB/s	460GB/s	819GB/s	1.2TB/s	≥ 2TB/s

Cap: x 64

BW: x16

Major update!

Notes: (1) HBM3P is Samsung's name for HBM3E; (2) HBMNext is Micron's name for HBM4, while its HBM3E is sometimes referred to as HBM3 Gen 2. (3) HBM3 technically supports 16Hi stacks, but so far, no manufacturer is using it. (4) Different from Samsung and SK hynix, Micron started manufacturing HBM2E with 1z DRAM. (5) Micron and SK hynix are expected to implement HBM3E with 1β/1b hynix) process, while Samsung is likely to start from the 1a process.

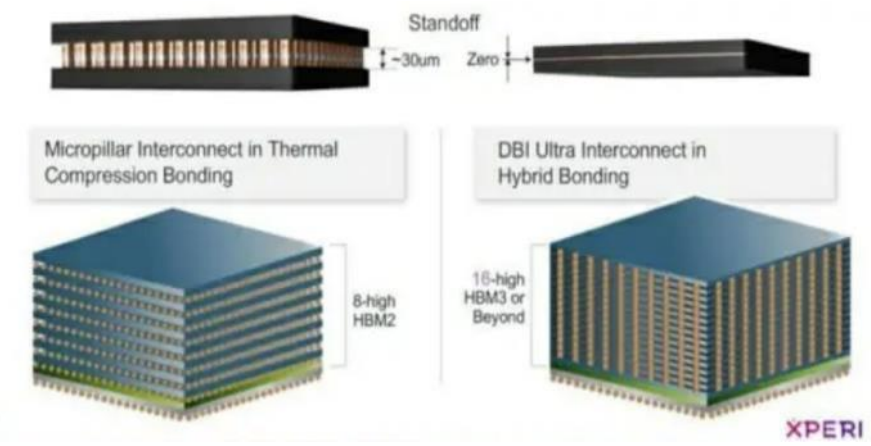
HBM – Technology Challenges

How To Increase Capacity?

Solution:
- Increase stack height

Limitation:
- Device height
- Heat dissipation

Change to max. 775µm allows 16-layer stacks with TCB *but does not solve the heat issue*



How To Increase Bandwith?

Solution:
- More parallel connections
- Higher clock rate

Limitation:
- Pin count
- Heat dissipation

Hybrid Bonding enables higher pin count and 20% better heat dissipation

Ultimately HBM will need Hybrid Interconnect Technology

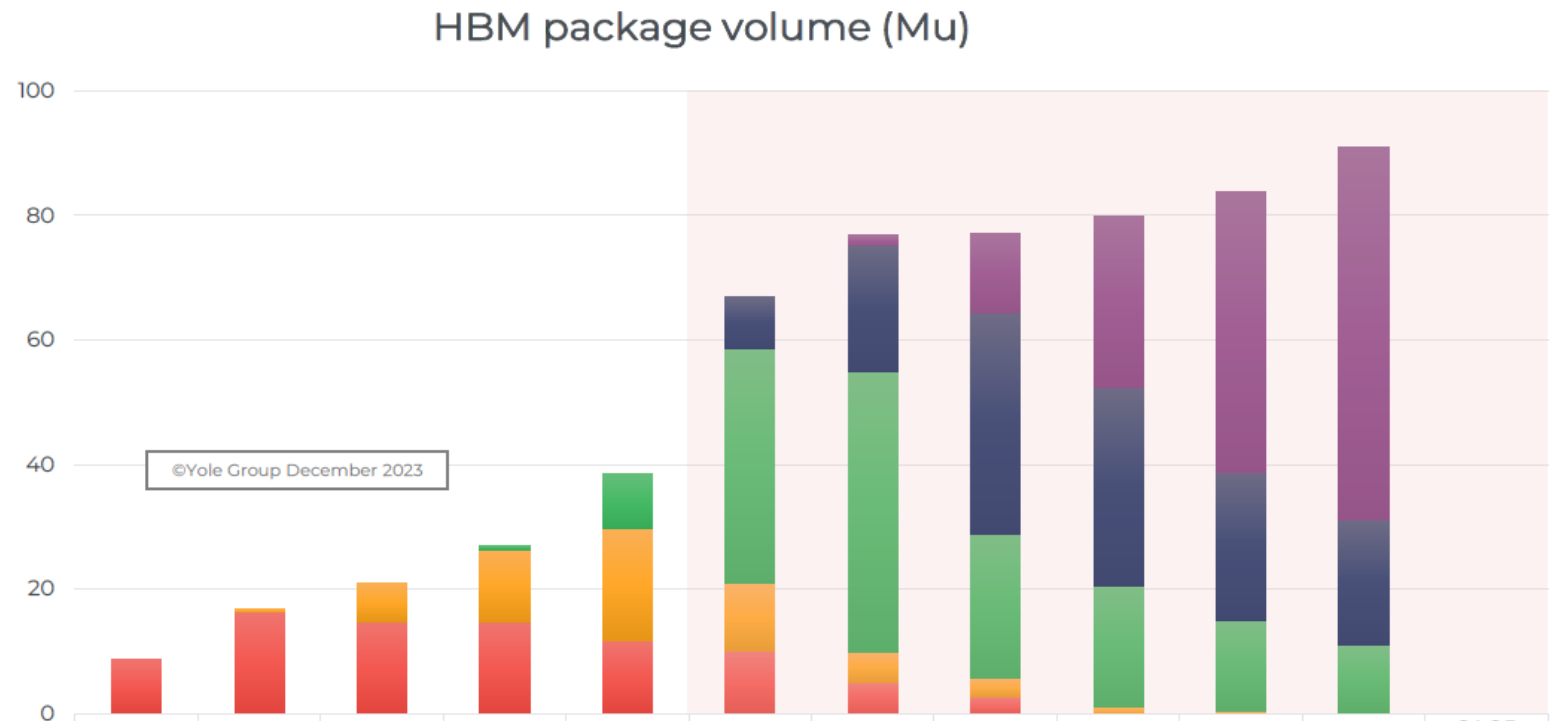
HBM Assembly Roadmap by Leading Producer

	Micron	Samsung	Hynix
HBM 3,3E 2024	NCF TC Non Conductive Film Thermo Compression	NCF TC Non Conductive Film Thermo Compression	MR-MUF Mass reflow Mold Underfill
HBM 4,4E 2026	Fluxless TC / Hybrid Working on both technologies	Fluxless TC / Hybrid Working on both technologies	Adv. MR-MUF / Hybrid Working on both technologies
	This HBM generation will see different technologies. Hybrid will be applied to 16 high stacks first.		
HBM 5+	Hybrid Highest number of contacts, stack height and thermal dissipation	Hybrid Highest number of contacts, stack height and thermal dissipation	Hybrid Highest number of contacts, stack height and thermal dissipation

HBM 4e/5 Production Expected to Accelerate in 2026

HBM PACKAGE* VOLUME – MARKET FORECAST

The volume of HBM packages (or stacks) is expected to grow at a $CAGR_{23-29}$ ~ 15%. The slower pace compared to wafer production (see next slide) is due to the rising average capacity per package.



	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	CAGR 23-29
HBM4 (and beyond)							1.6	12.9	27.6	44.9	59.9	
HBM3E						8.3	20.2	35.5	31.9	23.8	20.0	
HBM3				0.7	8.8	37.8	45.1	23.2	19.4	14.6	10.9	4%
HBM2E		0.5	6.1	11.7	18.0	10.9	4.9	2.9	1.1	0.4	0.2	-55%
HBM2	8.7	16.4	14.8	14.7	11.6	10.0	5.0	2.8				
Total	8.7	16.8	21.0	27.1	38.4	67.0	76.8	77.2	80.0	83.7	91.0	15%

Besi's TCB and Hybrid Bonding Systems Address Needs of Future HBM Interconnect Technologies

9800 TC next for ≤ 16 Stack HBM

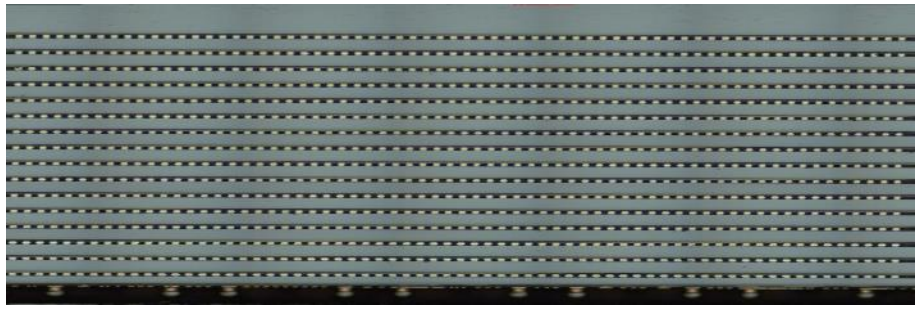
Micron

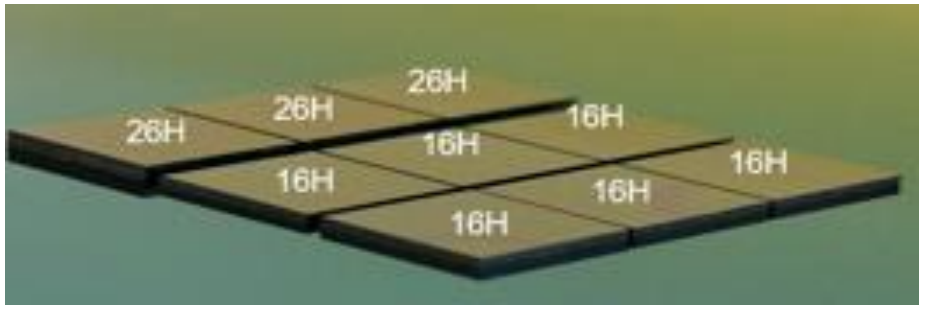
SAMSUNG

SK hynix

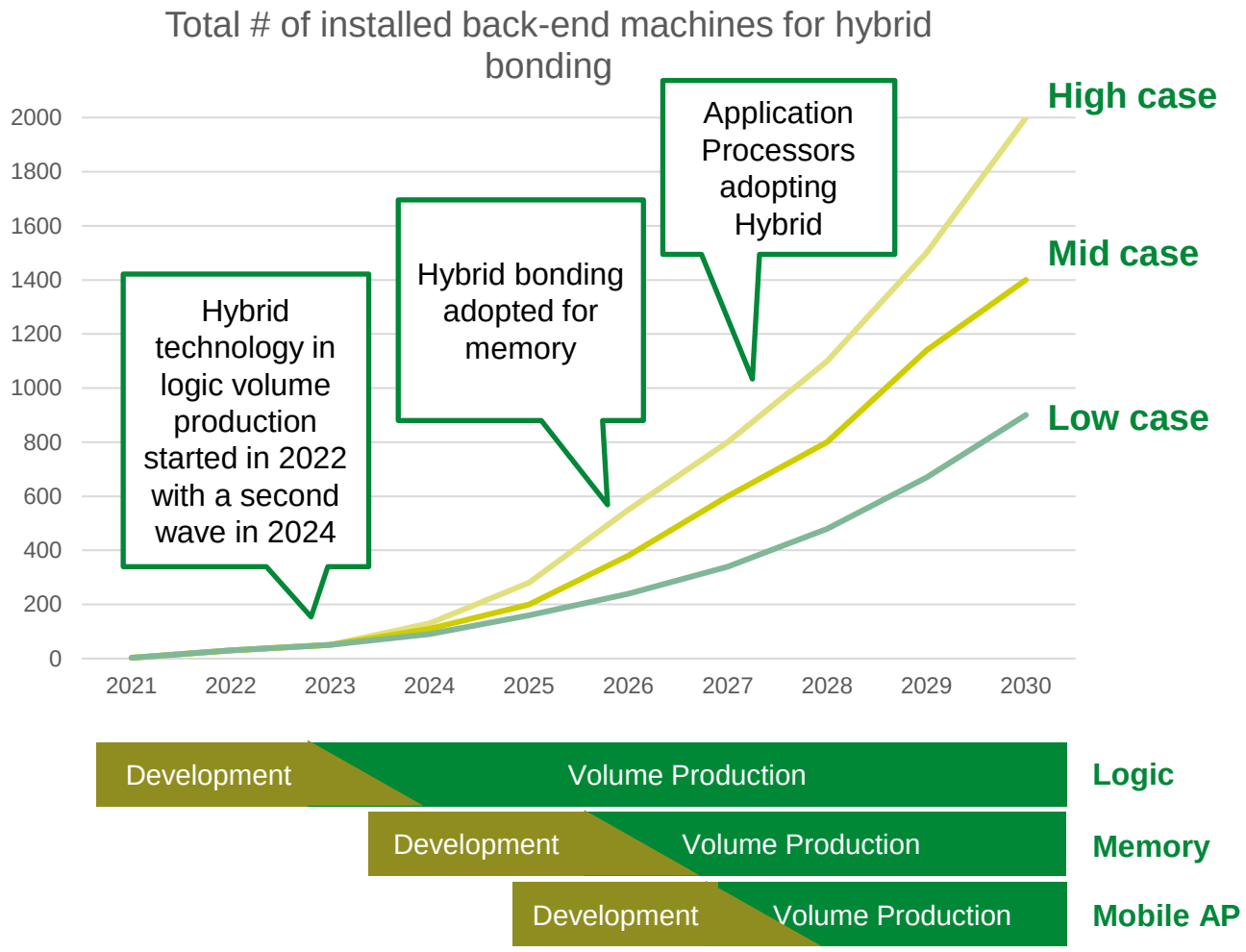
winbond

8800 Chameo ultra plus AC for ≥ 16 Stack HBM





Hybrid Bonding Market Potential – Logic and Memory Cases Confirmed



Source: Besi estimates, June 2024

Estimated 900 – 2,000 systems by 2030

Changes vs. Prior Forecast

- Market potential for each case increased 6% because of HB adoption expanding from 3-9 customers
- Logic adoption increased with 2nd customer in volume production and capex forecasts of leading players. TSMC projects 100% annual growth until 2026
- Memory adoption confirmed but shifted out one year
  - ➢ First Hybrid packaged HBM4(E) 16high stacks in 2026
- Edge AI driving hybrid adoption for mobile AP

Potential upside to estimates:

- Co-packaged optics
- Complex CMOS sensors

IV. MAINSTREAM DIE ATTACH
Christoph Scheiring
Senior VP Die Attach

Besi Die Attach Summary

Revenue	~80% of BESI
Market Share	~43%* Die Attach ~70% Advanced Die Attach
Market	Die Attach ~29% CAGR (2023-2026)*
Drivers	AI, CoWoS, Photonics, Mobile, Auto

- Source: TechInsights June 2024

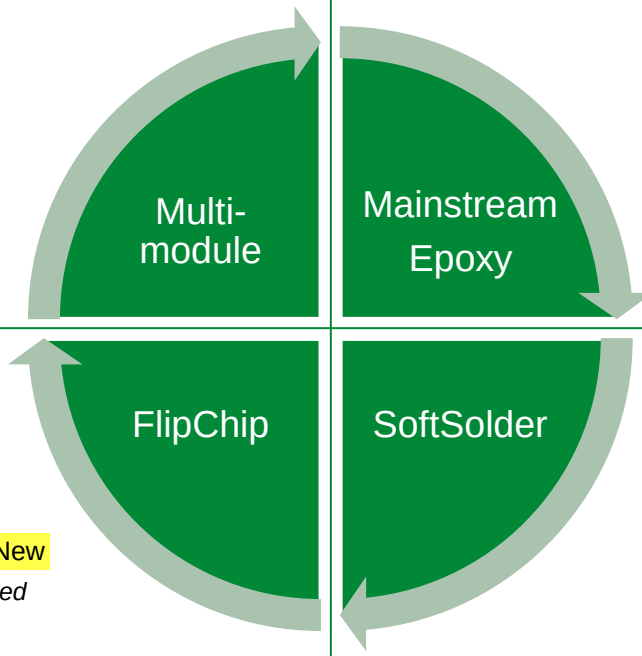
Industry Leading Die Attach Equipment Portfolio

Multi-Module Attach

- 2200 evo *advanced*
- 2200 evo *plus*
- 2200 evo
- 2200 evo hS
- 2200 evo hf

Die Bonding

- 2100 sD *advanced i*
- 2100 hS i
- 2100 hS ix
- 2100 hS



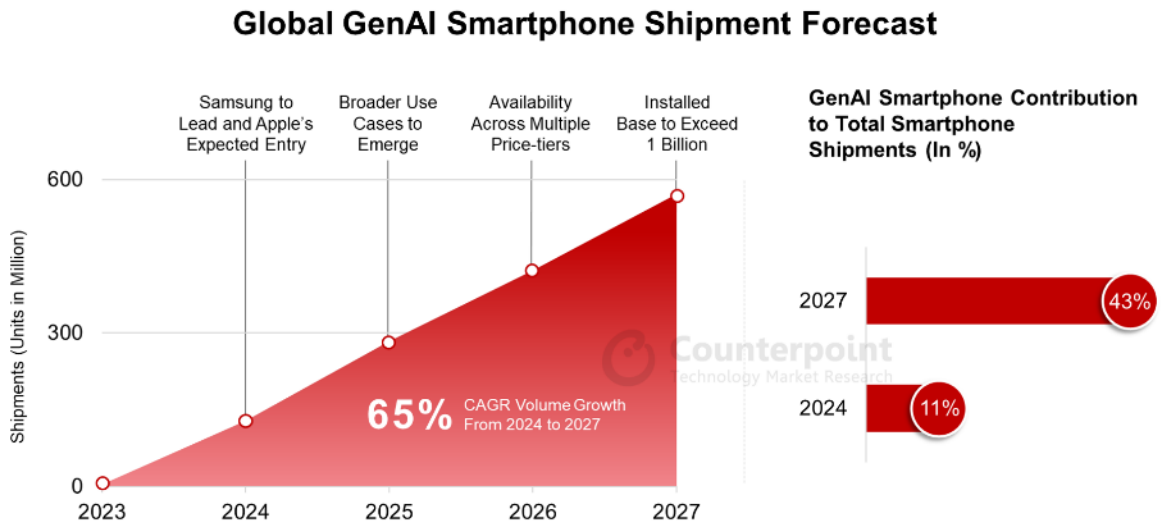
Flip-Chip

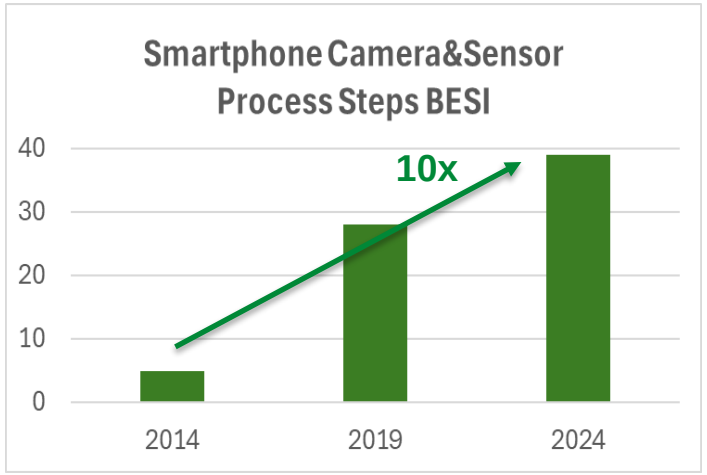
- 8800 CHAMEO *TnR* New
- 8800 CHAMEO *advanced*
- 8800 CHAMEO *Ultra*
- 8800 FC Quantum *adv*
- 8800 FC Quantum *hs*
- 2100 FC hS

Soft Solder

- 2100 SSI
- 2009 SSI

High End Smartphone Market Recovering
Future Growth Driven by AI Phones and New Camera Features





New Applications

- Variable aperture smartphone cameras
- Next level lens system assembly

Source: Xiaomi

Mobile

BESI SOLUTIONS

2200 evo advanced

8800 FC Quantum

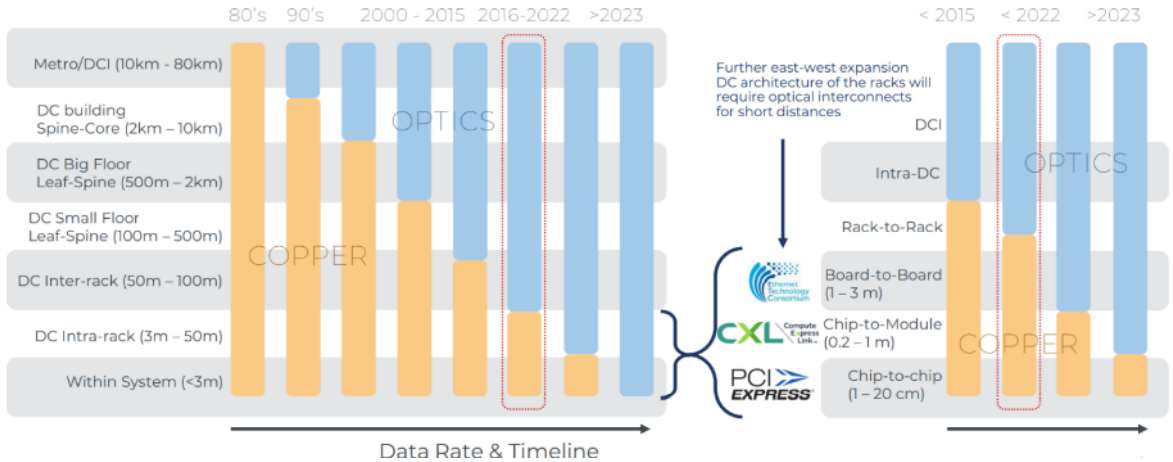
2100 hSi

- Fully Automated and Integrated Assembly
- Next generation cleanliness levels
- Advanced Inspection and process monitoring
- AI Camera systems

Industry Leading Photonics Platform in Rapidly Growing Market

Data Center Trends

- Electrical interconnects replaced by Optical interconnects
- Future: optical chip-to-chip connection CPO



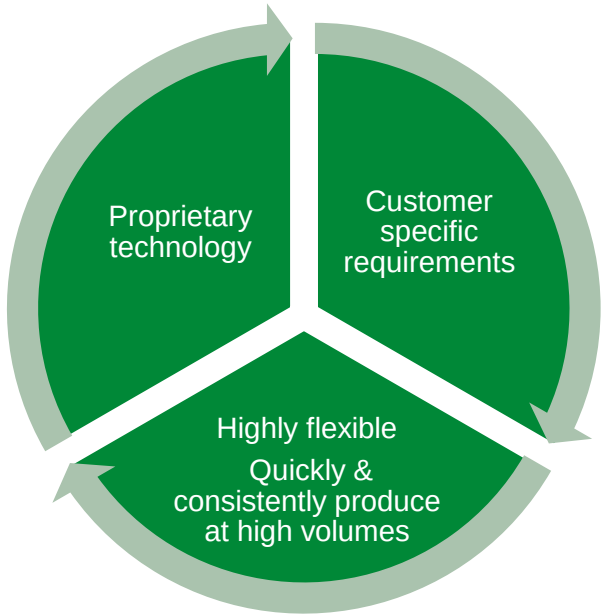
Source: Yole

Computer

BESI SOLUTIONS

Photonic – ROSA, TOSA, Laser, VCSEL assembly

- Ultimate process control & flexibility for complex system assembly
- Tailored solutions per customer



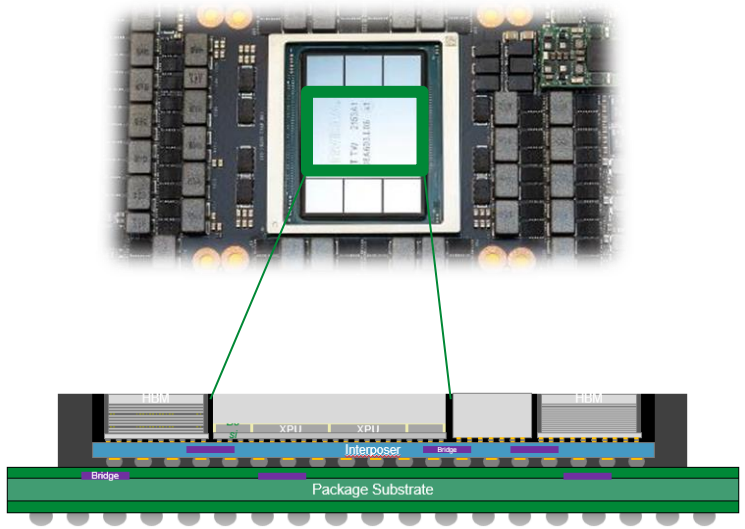
2200 Evo advanced

NEW

- Extend process portfolio with 1um accuracy (taking share of active alignment market)

Besi Portfolio Well Positioned to Take Advantage of Increased Investment in High Speed 2.5D CoW

Typical 2.5D assembly



NVIDIA
AMD
SAMSUNG
tsmc
QUALCOMM

Computer

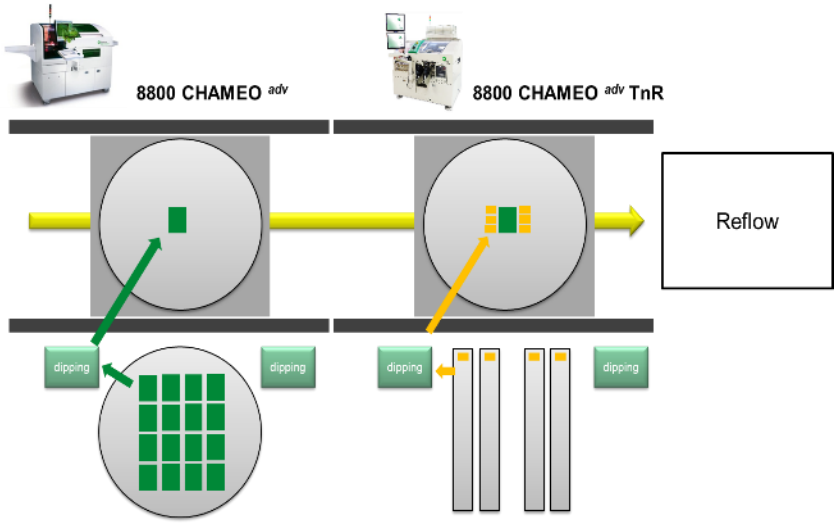
BESI SOLUTIONS

CoWoS – Unique High speed Integrated Logic and Memory Attach

- Introduced Q4 2023
- New High speed flip chip attach with dip fluxing
- Large dies up to 40x40mm
- Inline Wafer and T&R feeding for Logic and HBM attach

8800 Chameo advanced / TnR

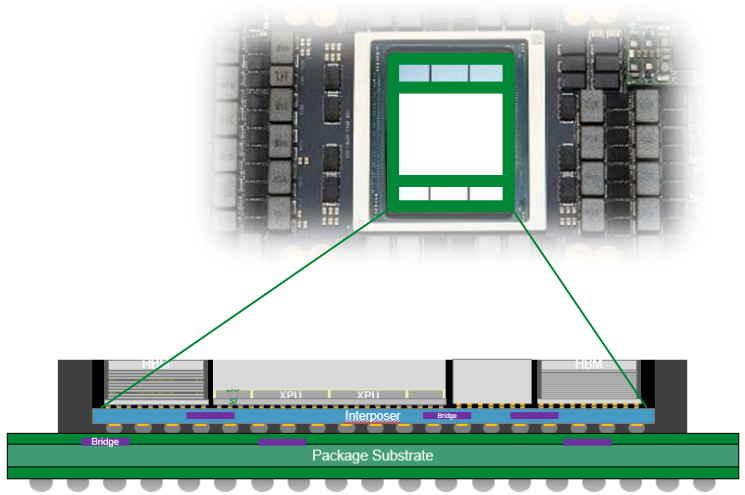
Logic Attach **HBM Attach**



NEW

- Moving from 3um to 1um accuracy

Besi's 2200 Evo Is Tool of Reference for Large Interposer CoW**oS** Flip Chip Attach



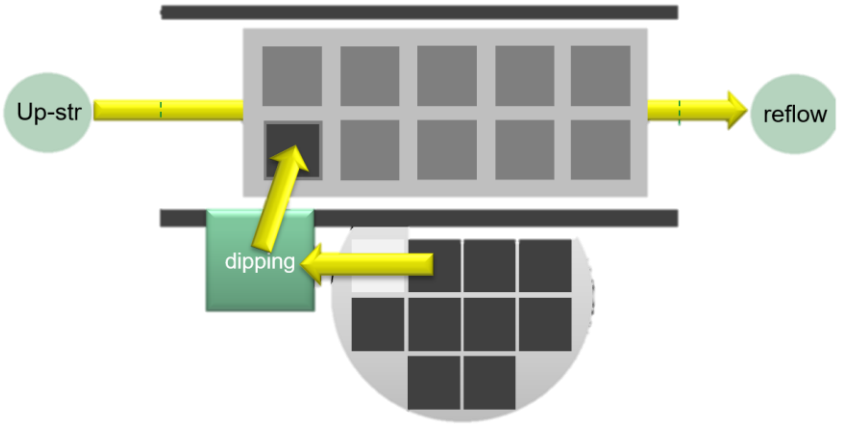
NVIDIA
AMD
SAMSUNG
tsmc
QUALCOMM

Computer

B E S I S O L U T I O N S

CoW**oS – Interposer Attach**

- Large die flip chip attach with dip fluxing
- Large die up to 72x72mm
- Inline or stand alone

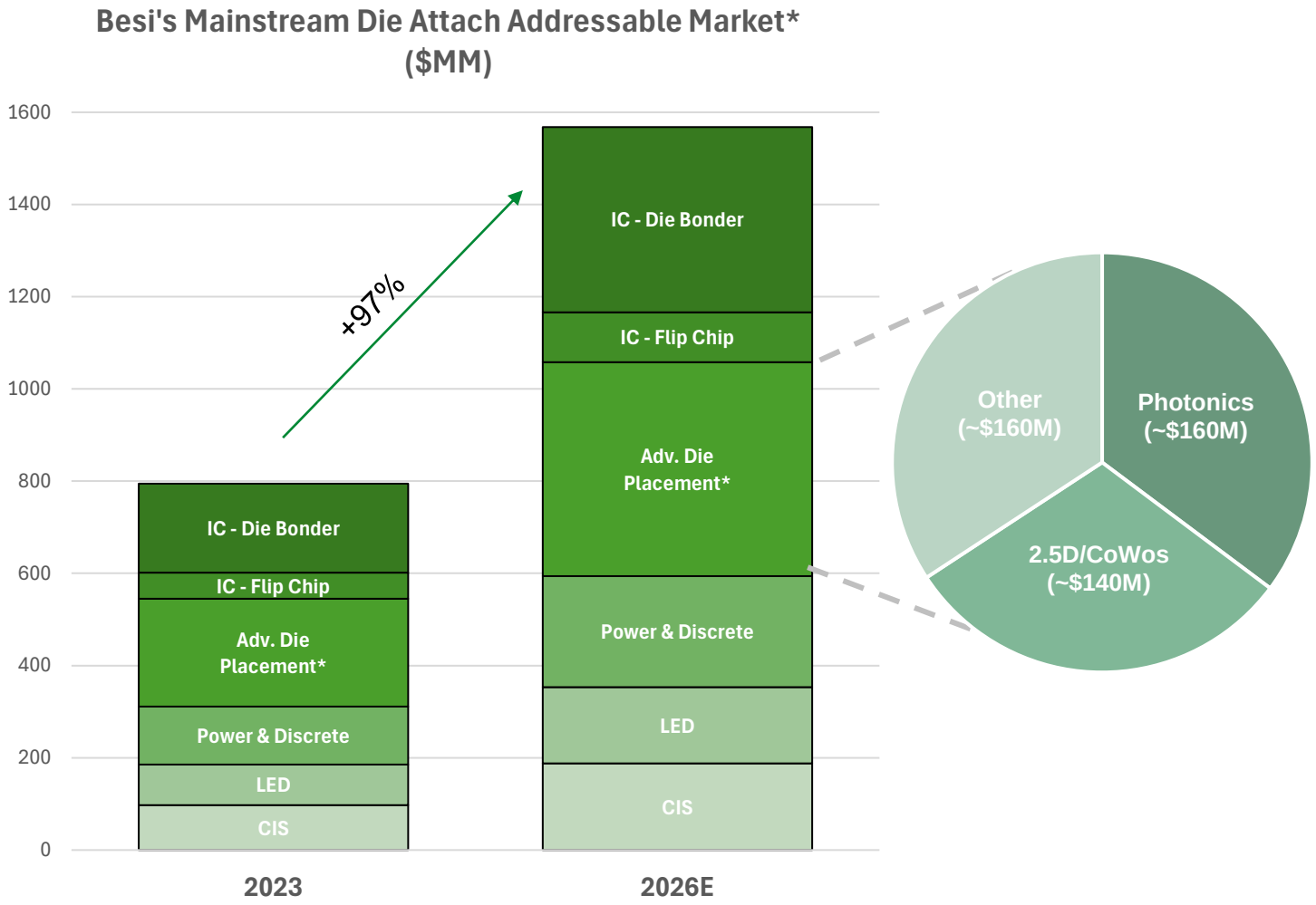


2200 Evo advanced

NEW

- Interposer size increasing to 120mm
- Adding TC & LCB bonding capability

Besi's Mainstream Die Attach Systems Well Positioned In Highest Growth Segments



Besi's mainstream addressable market expected to approximately double to $1.6B by 2026

Advanced Die Placement* represents large growth opportunity (+$230M) by 2026

- Photonics & 2.5D/CoWos fastest growing
- AI major driver

* Defined as <7 micron placement accuracy. Excludes hybrid bonding & TCB.
Source: TechInsights June 2024

VII. Q&A