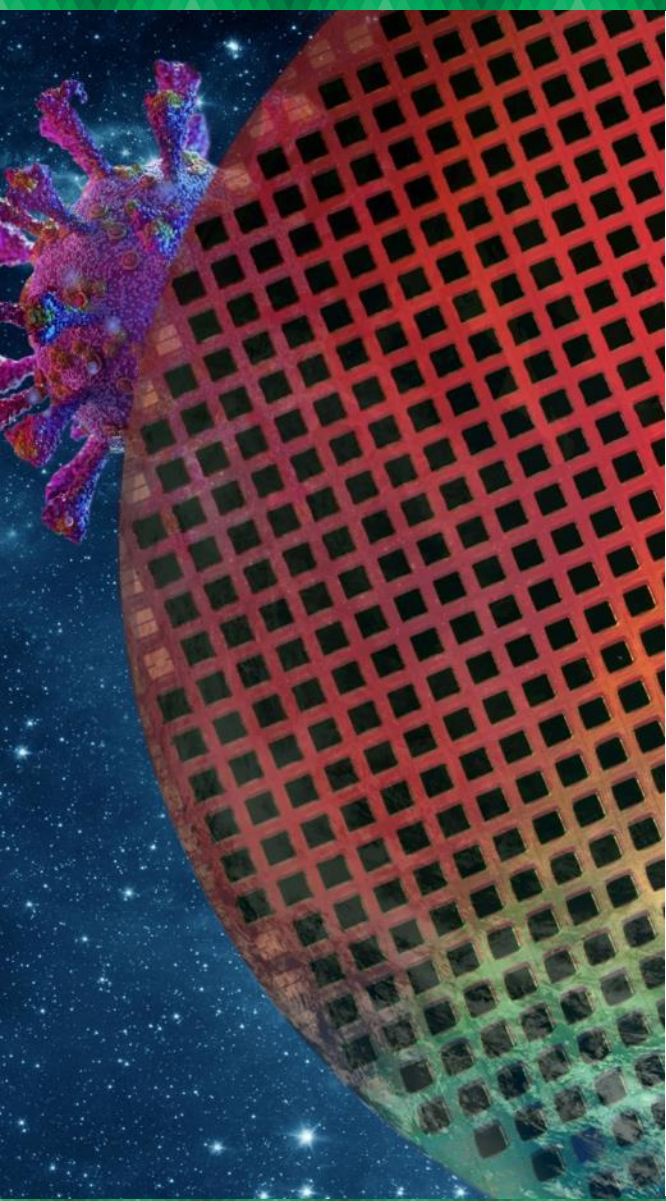




Besi Hybrid Bonding Presentation

March 2022

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward-looking statements, which are found in various places throughout the press release, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward looking statements, although not all forward looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward looking statements. While these forward looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 pandemic and measures taken to contain the outbreak, and the associated adverse impacts on the global economy, financial markets, and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region; potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers as a result of the COVID-19 pandemic; those additional risk factors set forth in Besi's annual report for the year ended December 31, 2021 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.



- Overview
- Hybrid Bonding Opportunity
- Q&A

Richard Blickman, CEO

Ruurd Boomsma, CTO

- Semiconductor assembly has moved from individual chip component circuitry to integration on chip level via hybrid bonding. Gating item for semiconductor development
- Hybrid bonding adoption has become most critical element to increasing circuitry speed and further reducing cost
- Has potential to become leading technology for <7nm nodes
- Will coexist with TCB/advanced flip chip and drive growth of high end assembly equipment market
- All leading semiconductor producers evaluating technology
- Market has potential to significantly exceed initial expectations
- Besi has a leading position with competitive advantage

Status Today

- Initial proof-of-concept orders received in Spring 2021
- Additional orders received in both Q2 and Q3-21 for delivery in H1-22
- Shipments Commenced in Q4-21
- Cluster tools available in Q2-22 to help support volume production
- Multiple customer engagements

Capacity/Support Expanded

- Expanded R&D teams in Europe and Singapore
- Added clean room production facilities in Malaysia and Austria (2021)
- Building capacity to produce 12-15 systems per month
- Engineers and software developers hired for US and Taiwan support

Agenda



- Overview
- Hybrid Bonding Opportunity
- Q&A

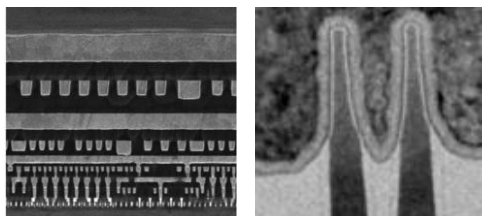
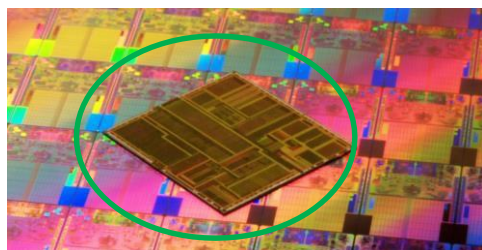
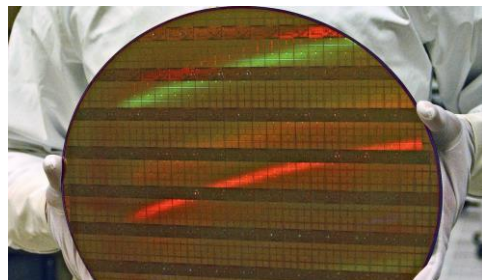
Richard Blickman, CEO

Ruurd Boomsma, CTO

Semiconductor Value Chain

FRONT-END

CREATING ELECTRONIC
DEVICE ON SILICON WAFER
FROM SIMPLE DIODE
TO HIGHLY COMPLEX ICs



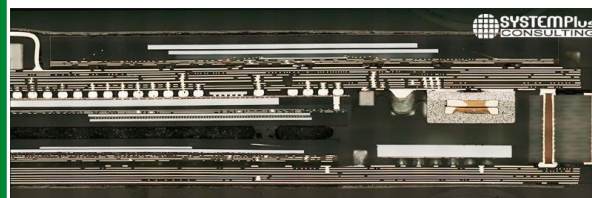
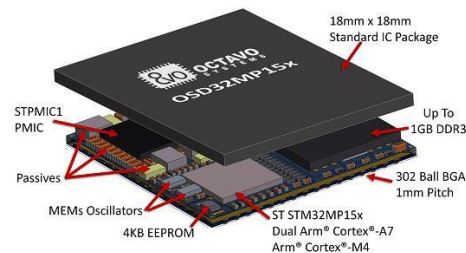
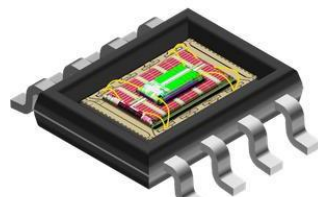
Source: Intel, Anandtech

nanometers

ASSEMBLY (BACK-END)



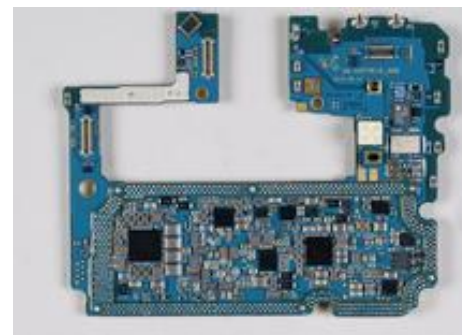
EQUIPMENT TO
PLACE DIES ON CARRIER
CONNECT TO OUTSIDE WORLD
PROTECTING THE DIE
COMBINING DIES IN PACKAGE



Source: Embedded, ST, System plus consulting

PCB

MOUNTING COMPONENTS
CONNECTING



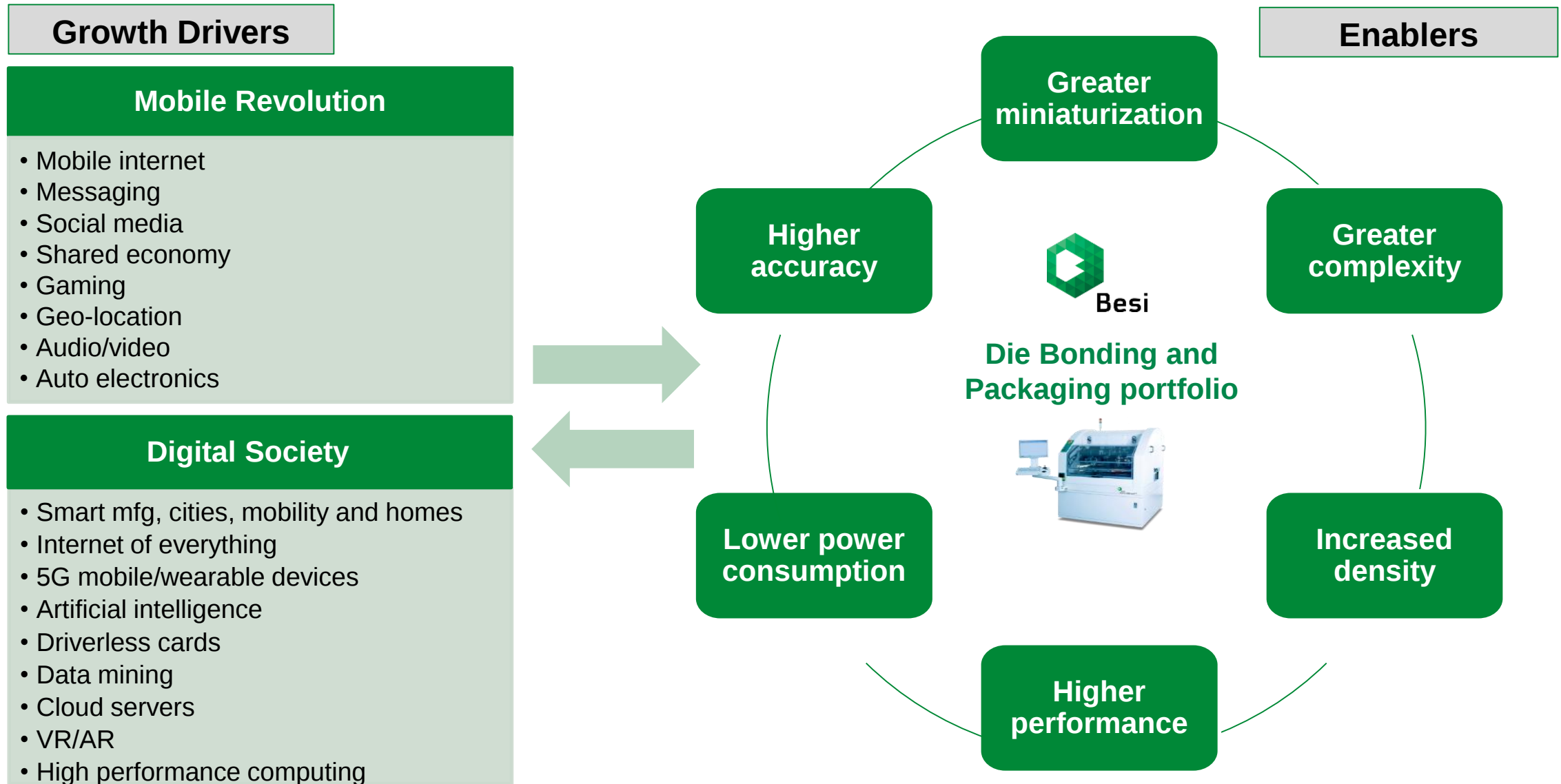
Source: Techinsight

END PRODUCT

ALMOST ALL PRODUCTS
BASED ON OR CONTAIN
ELECTRONIC DEVICES



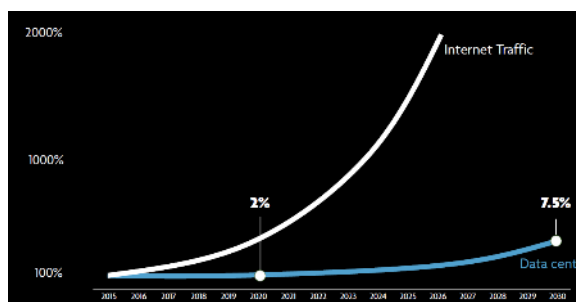
Advanced Packaging Critical to Next Generation Applications



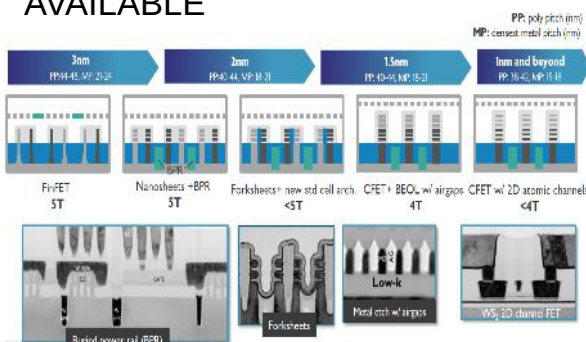
Growth in Advanced Packaging Will Continue as Gateway to Realizing Improved Performance in Next Gen Applications

Advancements in Miniaturization

SMALLER DEVICES ARE FASTER AND REQUIRE LESS ENERGY PER SWITCHING ACTION

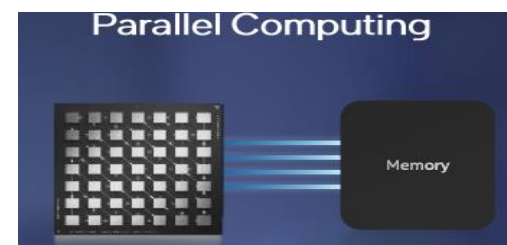
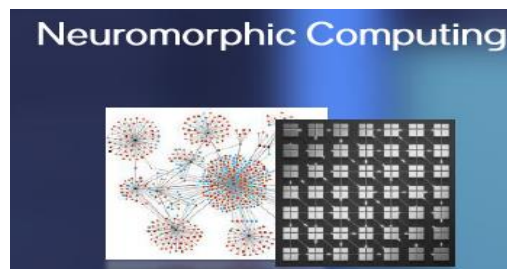


TECHNOLOGY ROADMAPS AVAILABLE

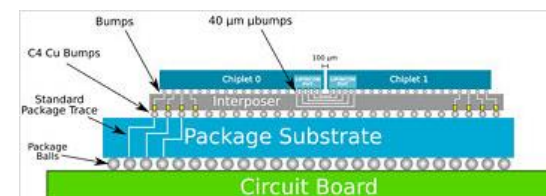


Source: IMEC

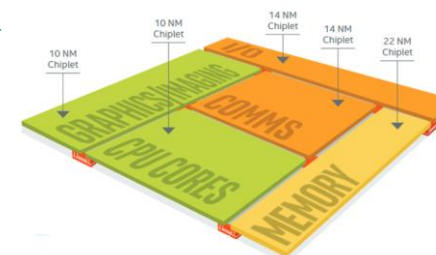
New Computing Methods



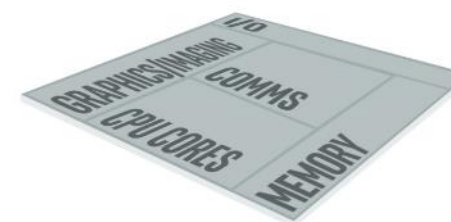
New Packaging Methods: Chiplets / 2.5 D Stacking



Multiple Smaller Stacked Dies

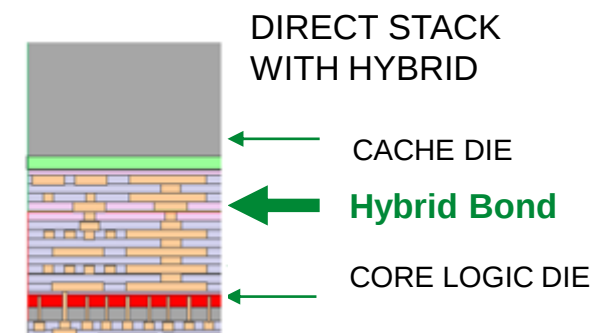


Multiple Smaller Dies Need more die attach process steps

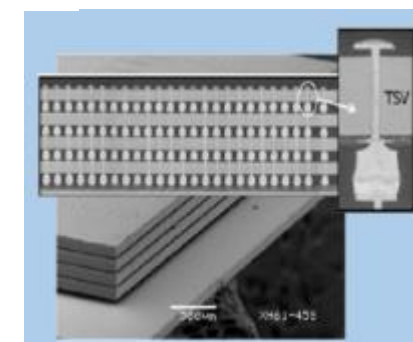


Single large Die

Real 3D Device Coupling With Die Stacking



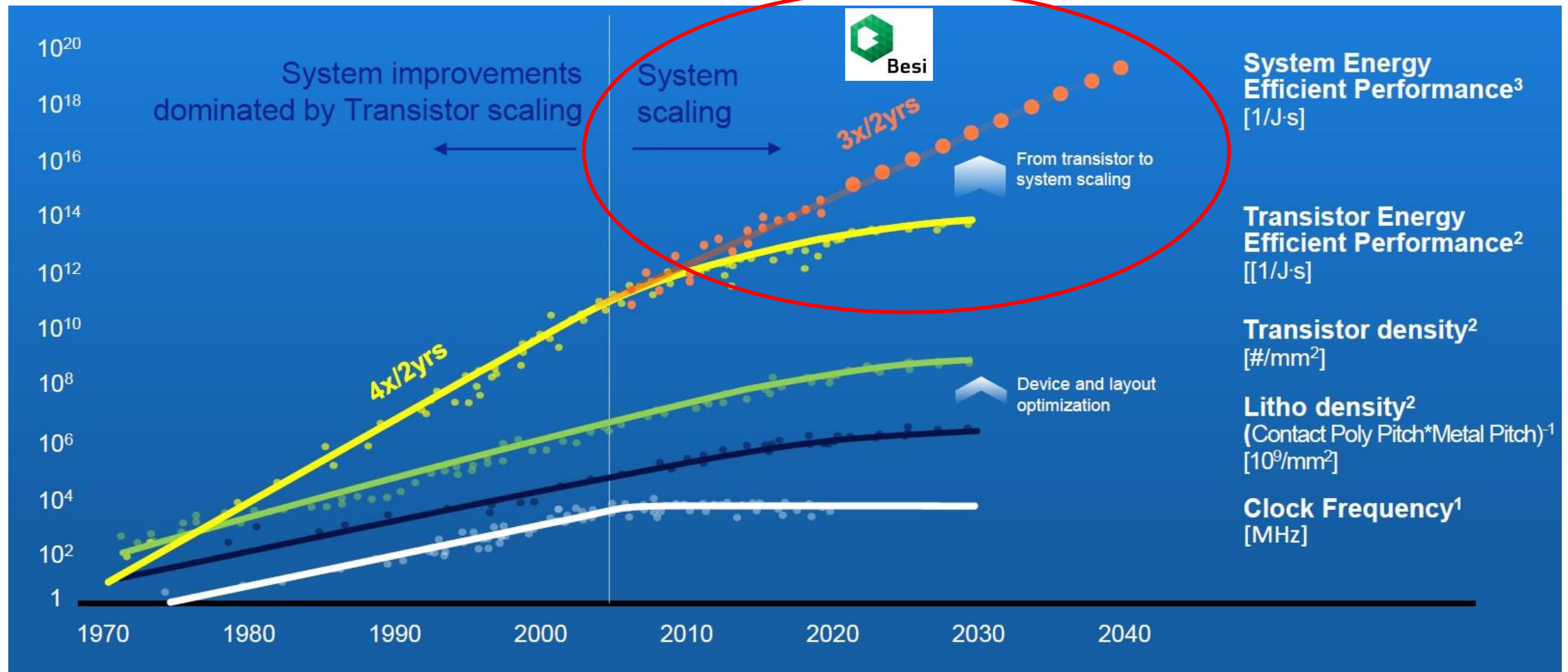
Besi



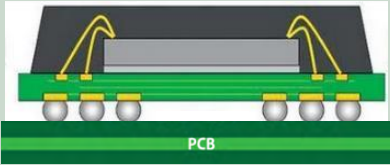
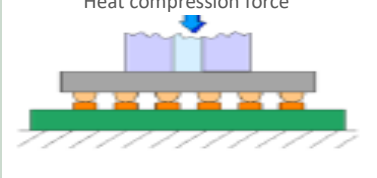
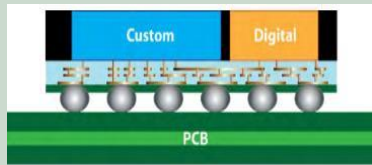
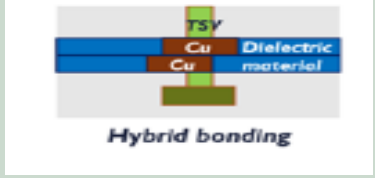
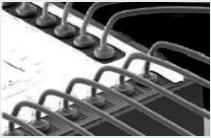
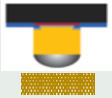
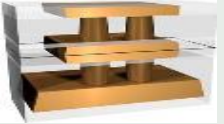
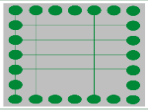
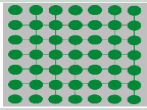
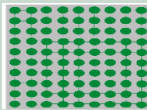
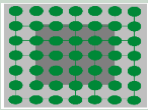
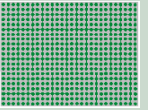
3D Stacking with TCB

Moore's law evolution: the next decade

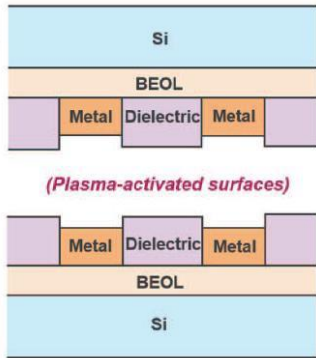
System scaling to satisfy the need for performance and energy consumption



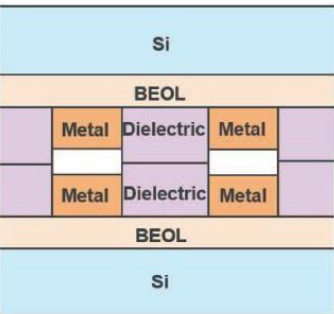
Moore's Law Helps Drive Growth of Wafer Level Assembly

	Wire Bond (1975)	Flip Chip (1995)	TCB Bonding (2012)	HD Fan Out (2015)	Hybrid Bonding (2018)
Architecture					
Contact Type	 Wire	 Solder ball or copper pillar	 Copper pillar	 RDL or copper pillar	 Copper to copper
Contact Density	 5-10/mm ²	 25-400/mm ²	 156-625/mm ²	 500+/mm ²	 10K-1MM/mm ²
Substrate	Organic/leadframe	Organic/leadframe	Organic /Silicon	None	None
Accuracy	20-10μm	10-5μm	5-1μm	5-1μm	0.5-0.1μm
Energy/Bit	10pJ/bit	0.5pJ/bit	0.1pJ/bit	0.5pJ/bit	<.05pJ/bit

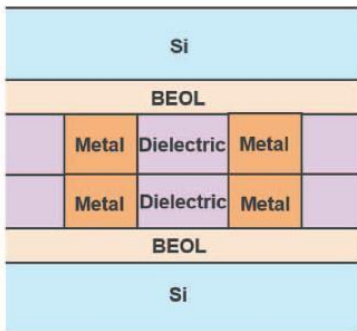
Understanding Hybrid Bonding



- 1 Preparation
 - CMP Polishing
 - Very flat < 5nm and clean
 - Surface Activation
 - Very Clean



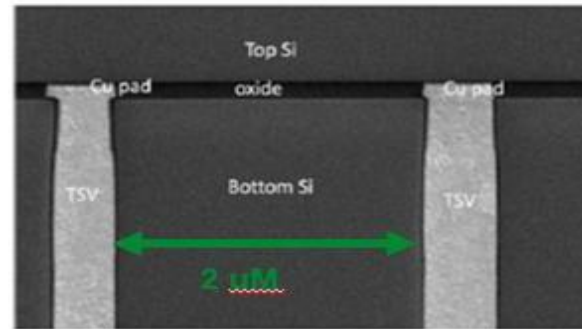
- 2 Bonding
 - Accurate Placement
 - Cold Bond
 - Based on initial dielectric bond



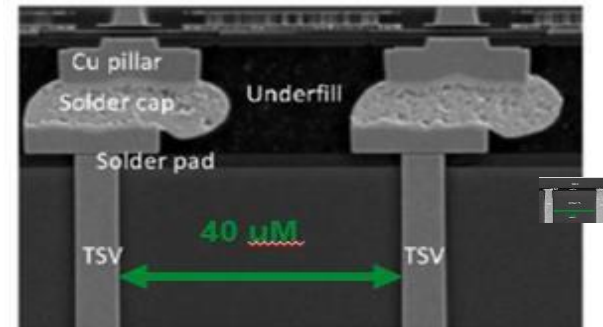
- 3 Cu-Cu Bonding via Anneal
 - Copper expands and contact is made
 - Depends on dishing
 - Depends on Cu properties

Die to Wafer and Die to Die Bonding of Chiplets

DIRECT CU-CU BOND

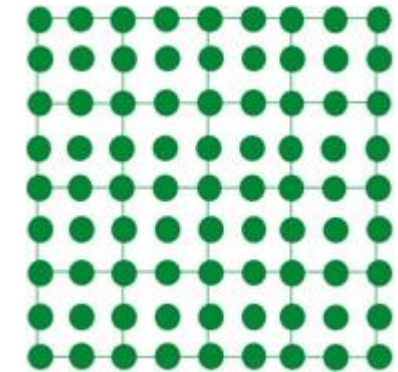
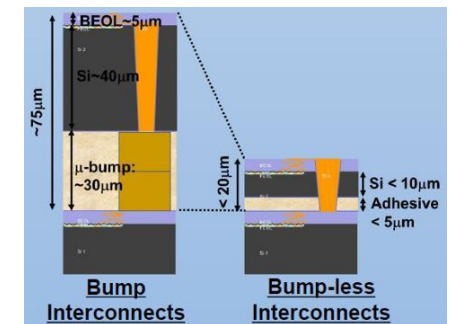


Compare to TCB



Source: XPERI ECTC 2019

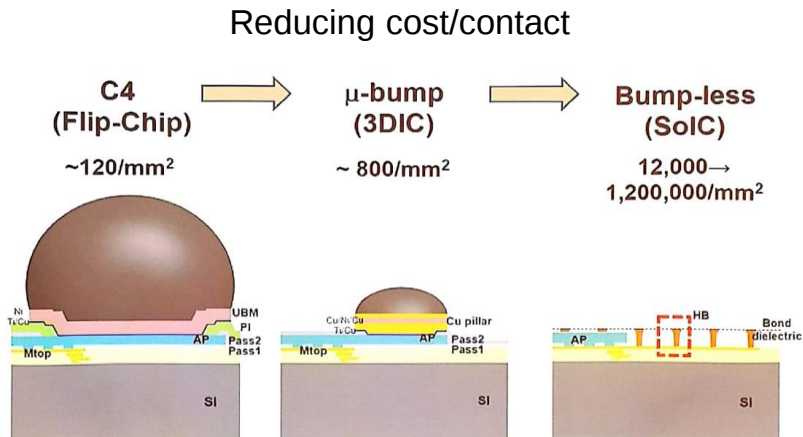
BUMPLESS INTERCONNECT



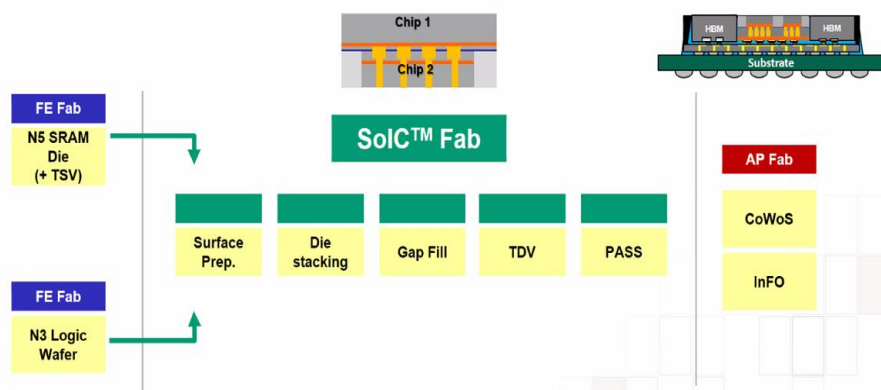
Used below 10 μm Pitch
and contact ! < 200nm Accurate

Merges Front-End/Back-End Processes

Requiring Much Smaller Dimensions



Hybrid die to wafer bonding much like front-end fab

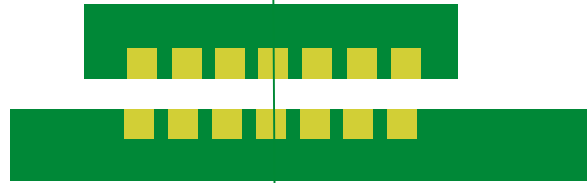


Source: TSMC

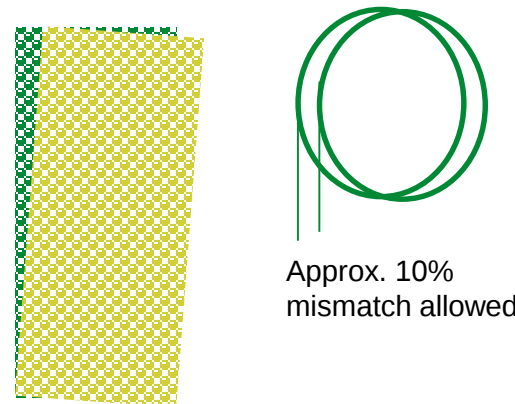
Requiring Much Higher Precision

Align Contacts
Very Precisely
In X and Y

Typical 10% Max
Deviation of contact size
1 μm contact $\Rightarrow$
100 nm Accuracy



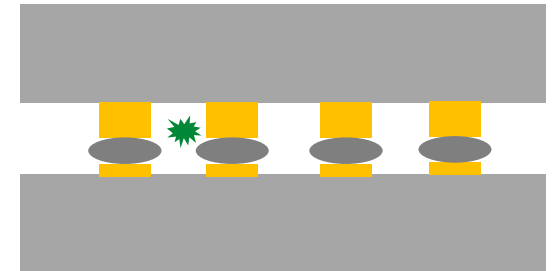
As well as angular control



1 μm Contact on 30 mm die
10% Mismatch at corner
3 mm on 1 km

Requiring Higher Levels of Cleanliness Comparable to Front-End Which Drives Upwards ASP

In TCB process, a small particle may have little effect

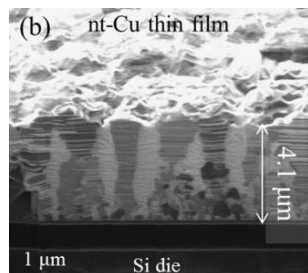


In hybrid process, a small particle may cause an open contact

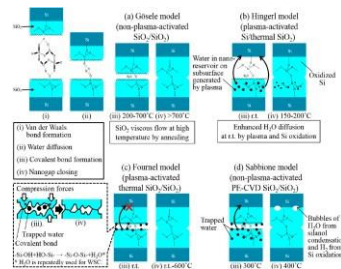


Many Front-End and Assembly Process Steps Involved in Clean Room Environment

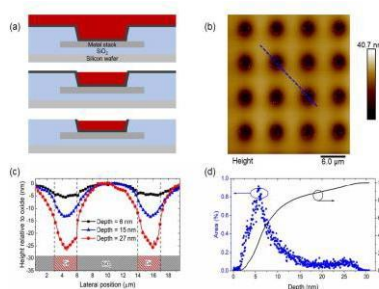
Copper quality and fill



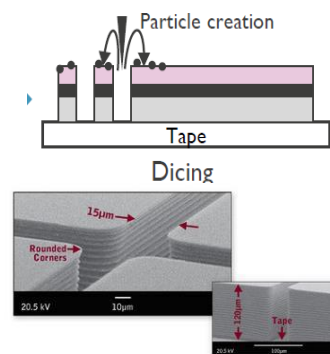
Impact of oxide deposition



CMP and Dishing



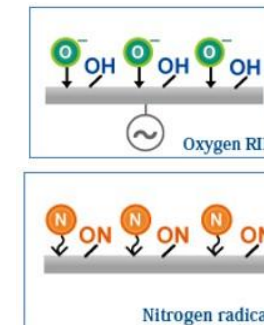
Dicing Cleanliness



Cleaning Parameters



Plasma Activation Parameters



Optimized Bonding Geometry

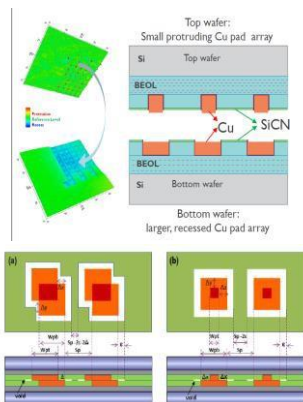
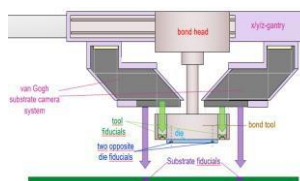


Figure 14. Cu pad design for hybrid wafer bonding: (a) equal pad size layout and (b) unequal pad size layout.

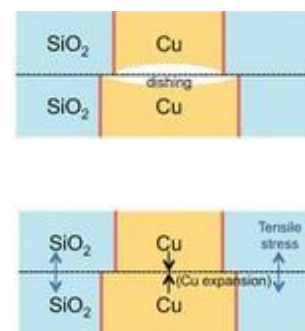
Bonding Process Industrial Solution



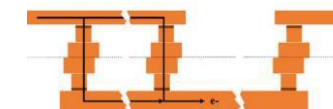
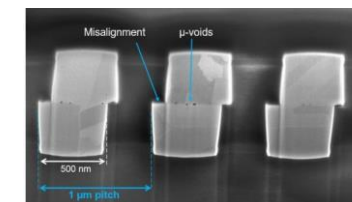
Integrated Process Flow Low Particles Inspection



Anneal

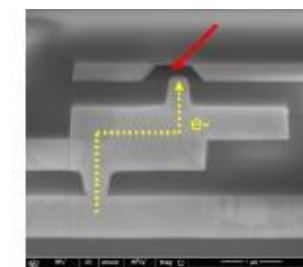


Electrical



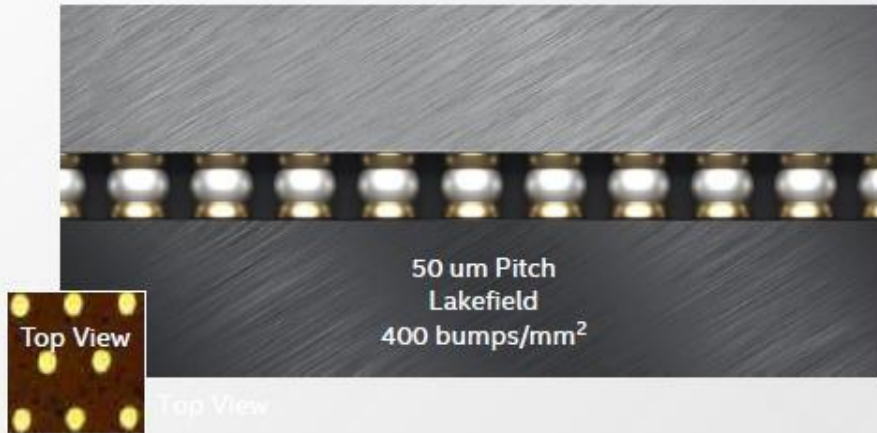
Life Time

- Corrosion
- Electromigration
- Thermal Stability



Hybrid Bonding is a Game Changer for Increasing Contact Density

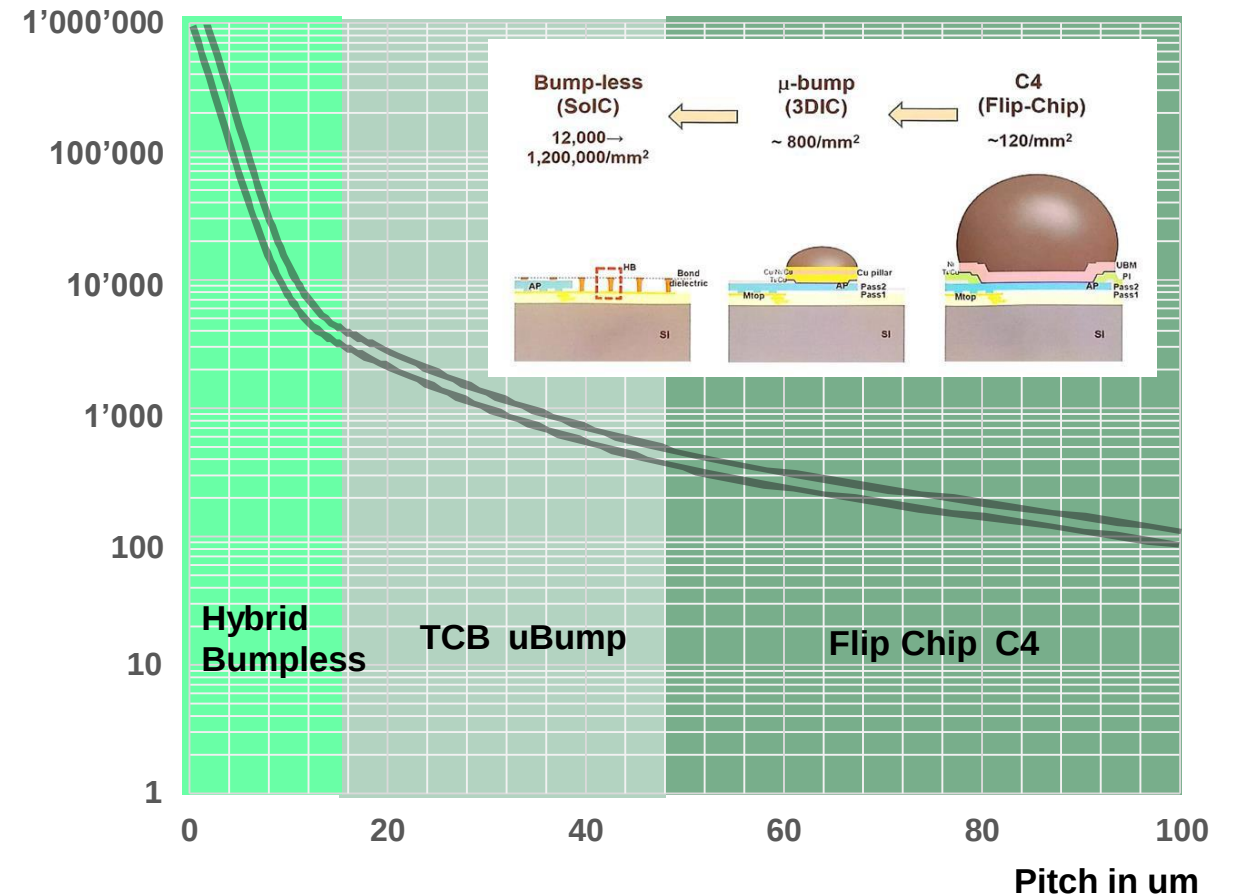
MORE DATA => MORE CONTACTS



Source: Intel

Contacts
Per mm²

Contact Density at Different Contact Pitches



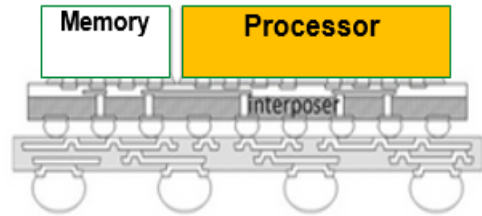
Requires More Process Steps Resulting in Higher Assembly Capital Intensity

Hybrid Bonding Adoption Will Generate Additional Demand For Assembly Equipment

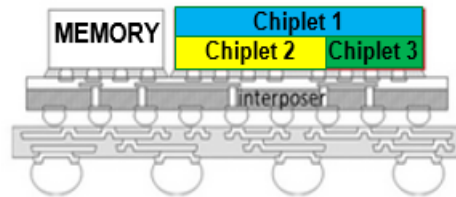
LOGIC

Example: COWOS TYPE STRUCTURE

Current Design
3 BONDING STEPS

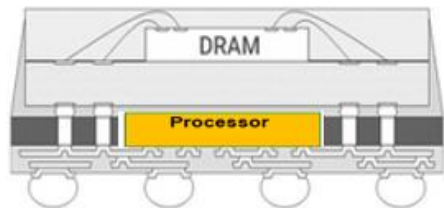


With Hybrid Bonding
5 BONDING STEPS

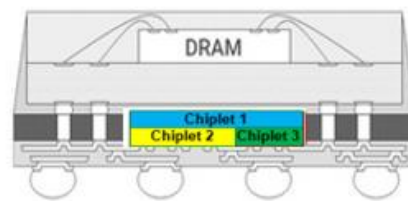


Example: FAN OUT TYPE STRUCTURE

Current Design
2 BONDING STEPS



With Hybrid Bonding
4 BONDING STEPS

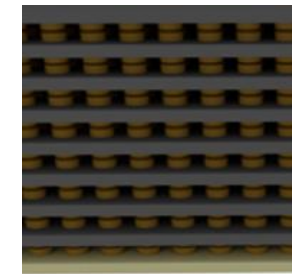


Source: TSMC

MEMORY

CASE 1 => HYBRID MAY REPLACE 1 TO 1 TCB

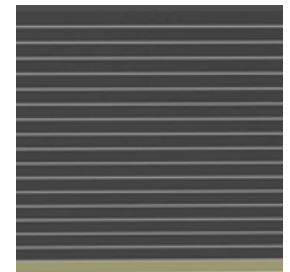
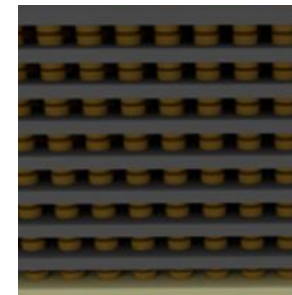
TCB BONDED HBM



HYBRID BONDED HBM



CASE 2 => HYBRID WILL ALLOW FOR MORE DIES IN SAME STACK HEIGHT LEADING TO MORE BONDING STEPS

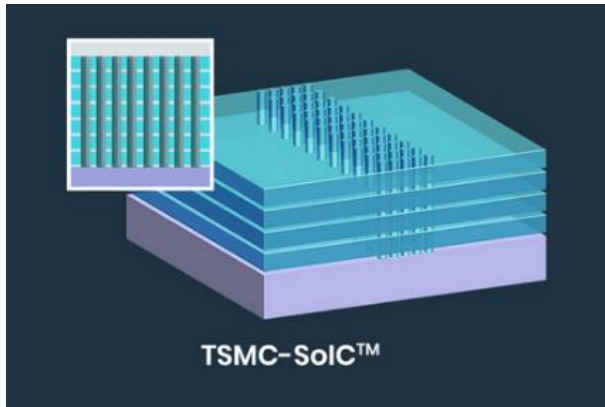


Source: Xperi

Now on Agenda of All Big Players



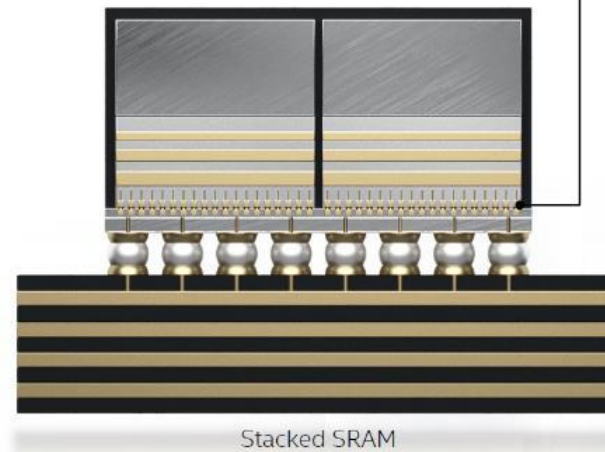
SAMSUNG



Hybrid Bonding

Enabling new architectures

TSV/Hybrid Bonding



Source: Intel Architecture Day 2020

Cu Hybrid Bonding Technology

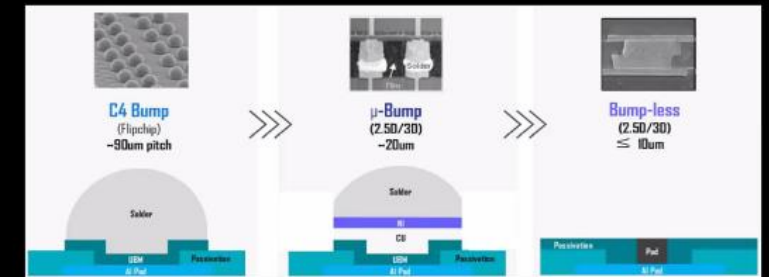
Bonding performance affects package performance *Electrical & thermal



Bandwidth	Bond Pitch	Allowable Power	Bond Gap
Up to 300% vs CuW	Up to 85% vs CuW	Up to 33% vs CuW	Up to 67% vs CuW

(source : IWLPC 2019, SAMSUNG)

Fine pitch requires continuously New Bump & Bonding Technology



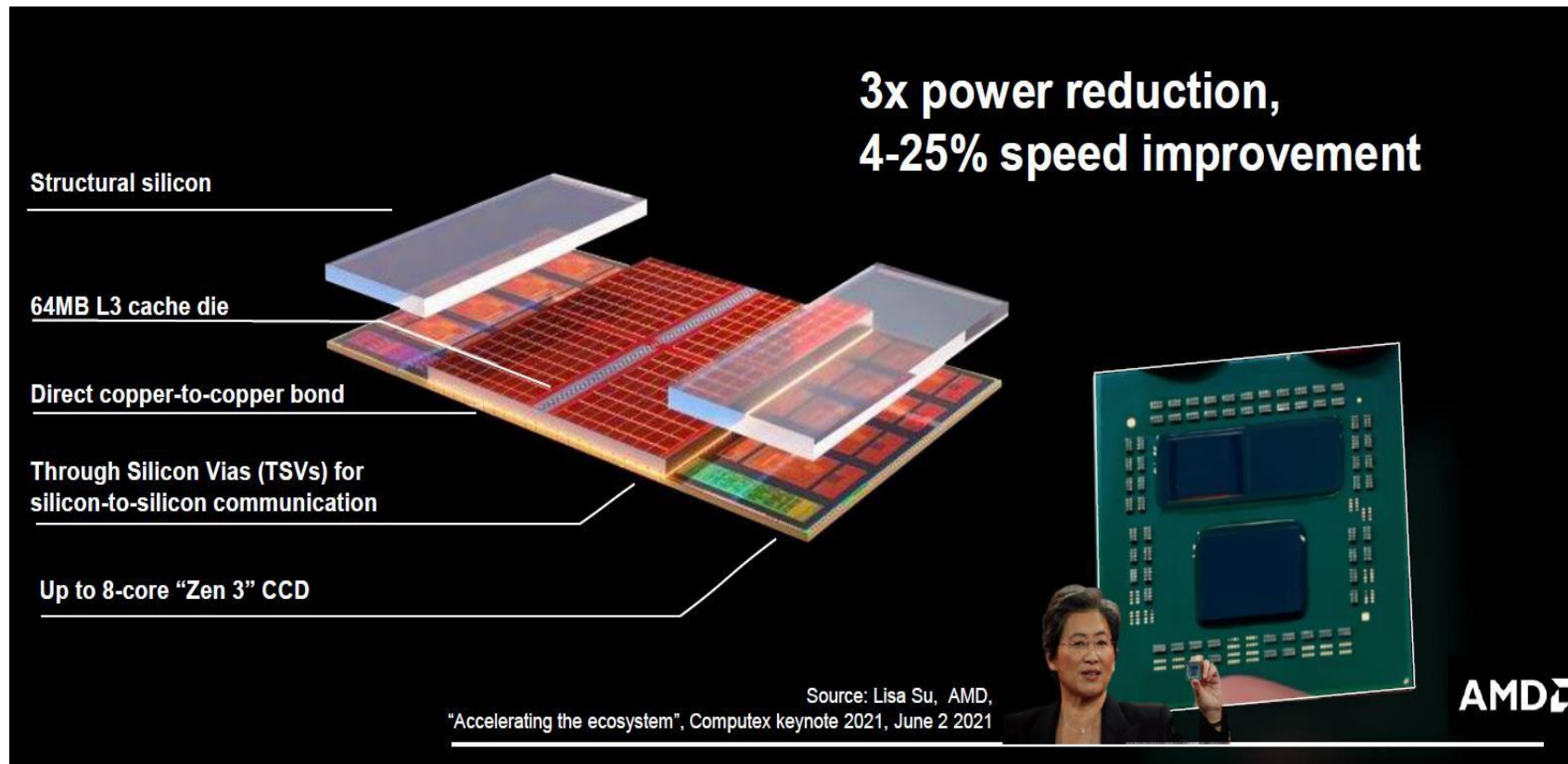
(source : SAFE 2020, SAMSUNG)

Source: Samsung presentations

Source: TSMC, AMD presentations

Chiplet Based System With Hybrid Connections is Next Step

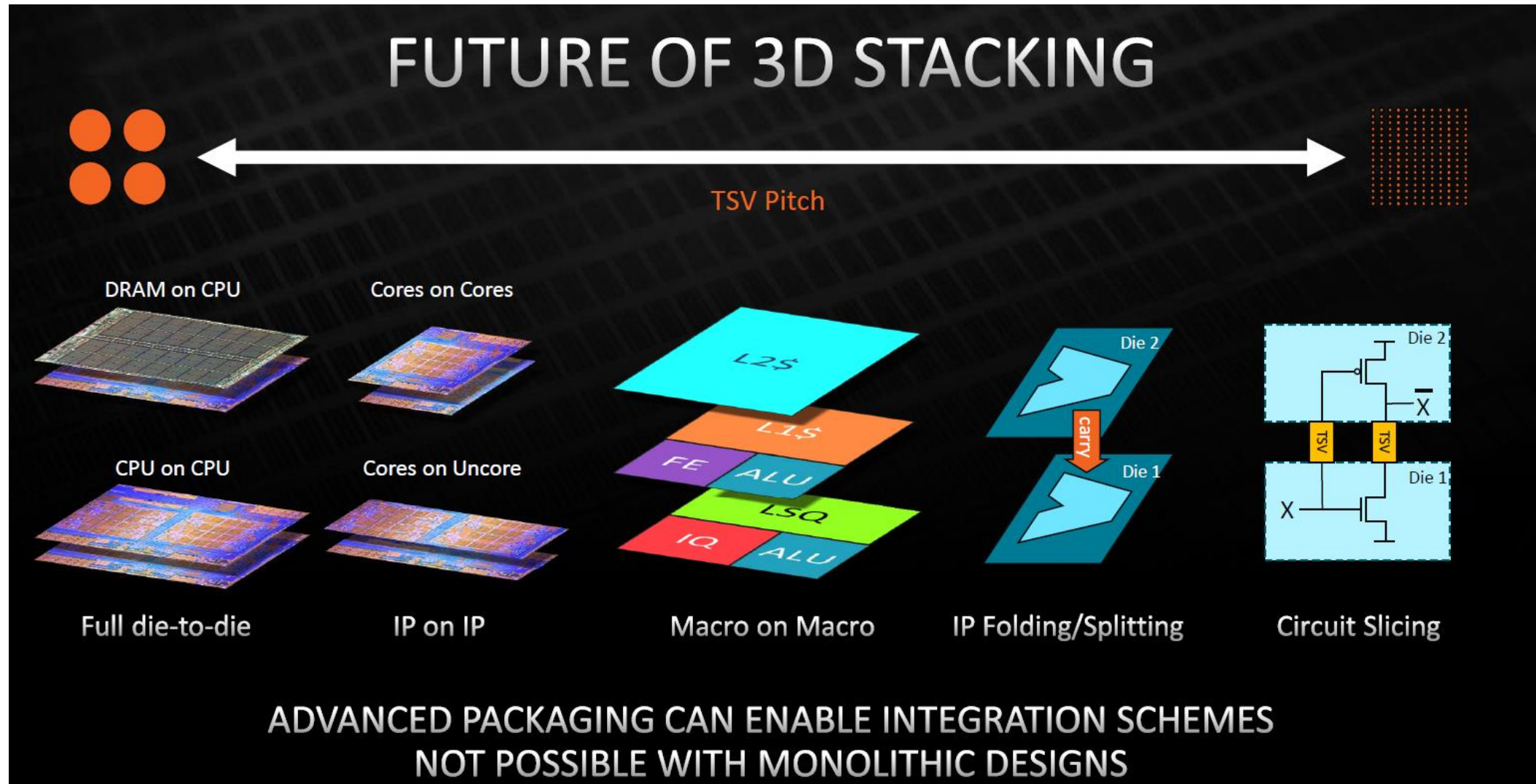
AMD 3D chiplet gives an 3.1-3.8 EEP improvement By integrating memory with the processor in one package



AMD EPYC Milan X

Announced November 2021
Eight CCD chiplets + I/O die
3D V-Cache using hybrid bonding





Source: AMD

Hybrid Bonding Adoption Leads to Higher Capital Intensity per UPH

8800 FC Quantum 3 micron accuracy



ASP: \$500k

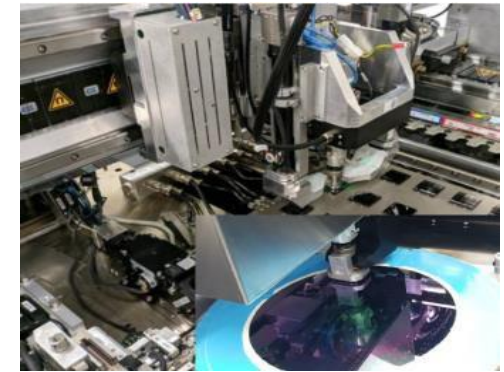
~9,000uph

8800 Ultra Accurate Chip to Wafer Hybrid Bonder <200 nanometer accuracy



Pricing: \$1.5MM-2.5MM
Configuration dependent

~1,500uph

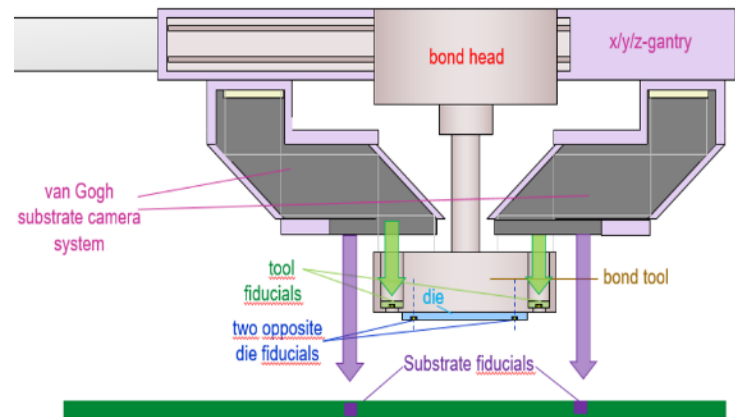


Status Update: Besi/AMAT Development Cooperation

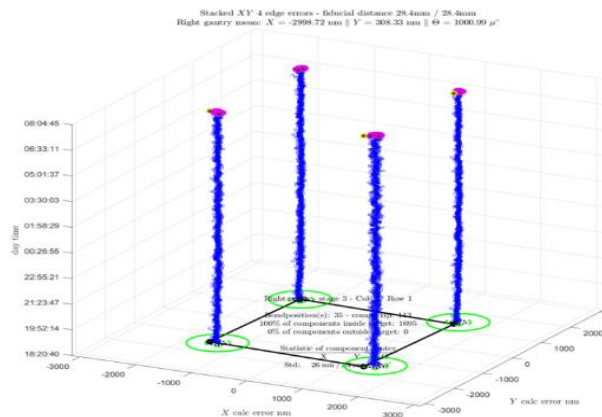


SYSTEM IMPROVEMENTS

REACHING 122nm ACCURACY
OUTPUT UP TO 2,000 UPH



High accuracy placement within 200nm radius



JOINT DEVELOPMENT COOPERATION AMAT AND BESI

ANNOUNCED OCTOBER 2020



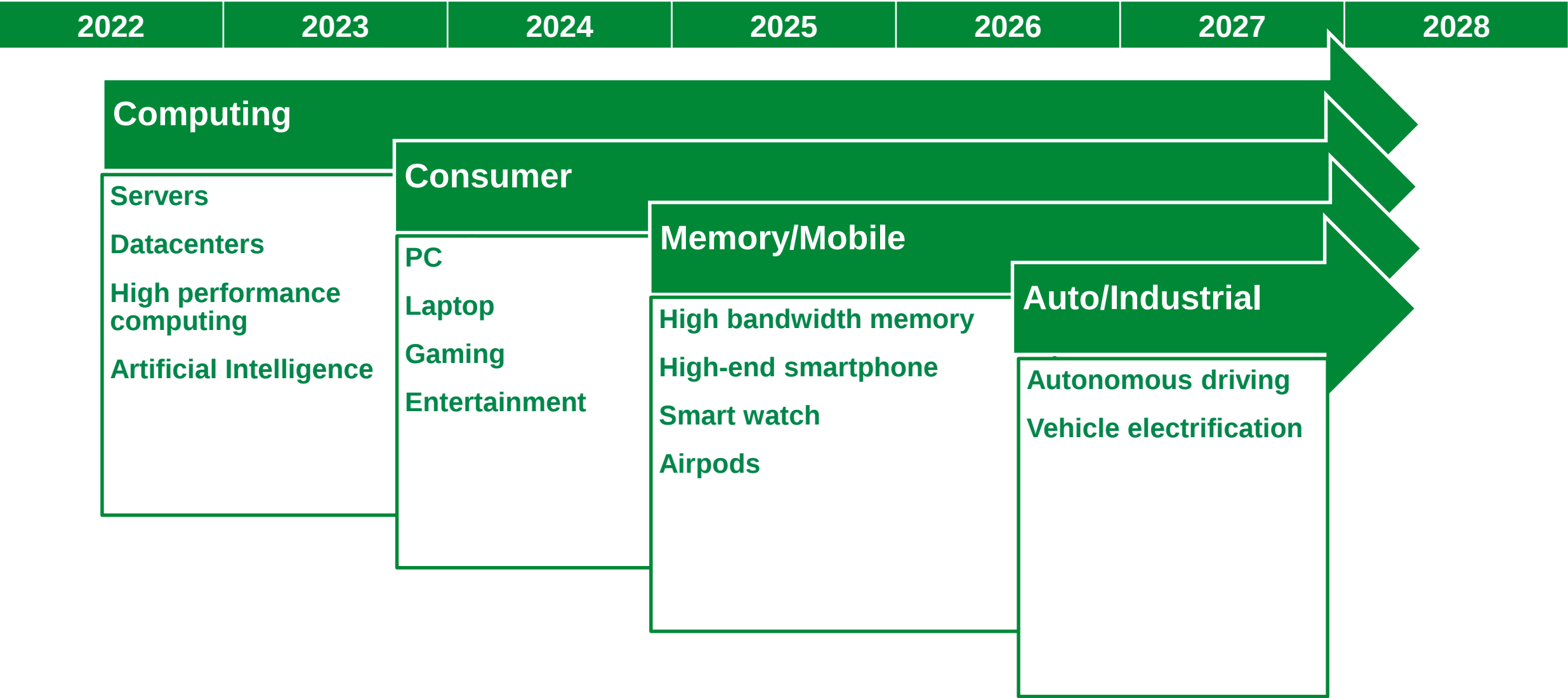
- Front and Back-End Process Expertise
- Dedicated Packaging Development Center
- Platform Design and Integration
- Assembly Equipment Process Expertise
- Market Leader in Hybrid Bonding Systems

JOINT HYBRID CENTRE IN SINGAPORE
JOINT DEVELOPMENT OF CLUSTER SOLUTION

SUBSTANTIAL INVESTMENT IN CLEAN ROOM INFRASTRUCTURE, MEASUREMENT EQUIPMENT, AND PEOPLE



Estimated Timetable for Hybrid Bonding Applications



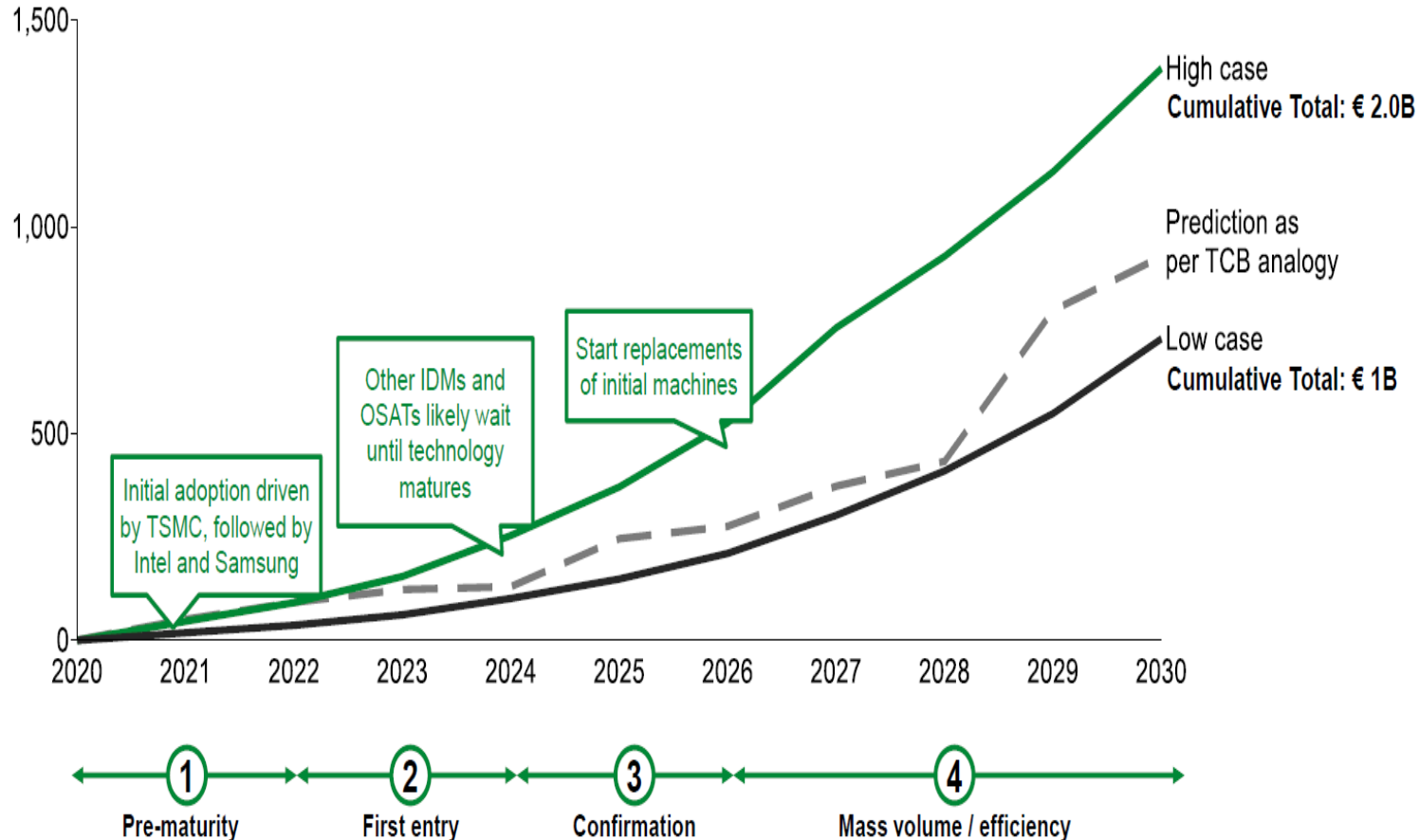
Hybrid Die Bonding Market Update

HYBRID BONDING

EQUIPMENT MARKET

June 2020 estimate

Total # of installed back-end machines for hybrid bonding



Source: Besii estimates

Market tracking above high case developed in June 2020

- High level of customer engagement
- Significant interest expressed by both logic and memory players
- Collaboration with AMAT enhances market position
- AMD first to announce hybrid bonded 3D chiplet-based processor
- Building capacity to € 300-400MM/annum
- **Full adoption by high-end smartphone manufacturers could significantly expand market opportunity**

Forecast highly dependent on timing of:

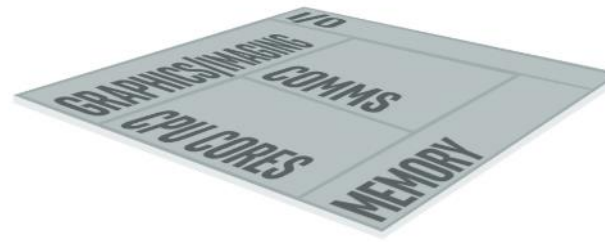
- Successful design and development per IDM
- Customer roadmaps
- Successful performance in mass production environment

Chiplet Adoption Enables Cost Effective Means of Increasing Performance

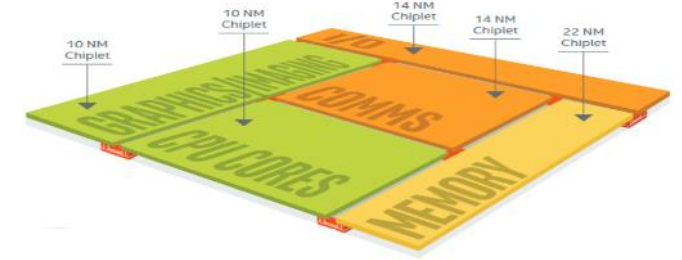
For many years the most direct way to improve capacity and performance was to increase wafer size and design by using smaller devices with more transistors/mm²

5 nm node seems to be the turning point where chiplet technology becomes more cost effective to further increase performance

Chiplet Adoption Also Increases Assembly Capital Intensity



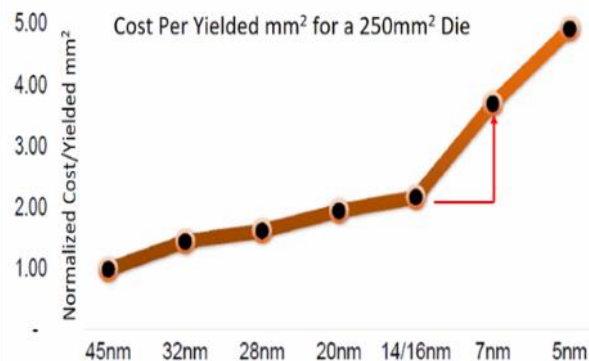
**Single Silicon Die
1 Die Bonding Step**



**Split into 5 smaller dies connected with
5 Bridges = 10 Die Bonding Steps!**

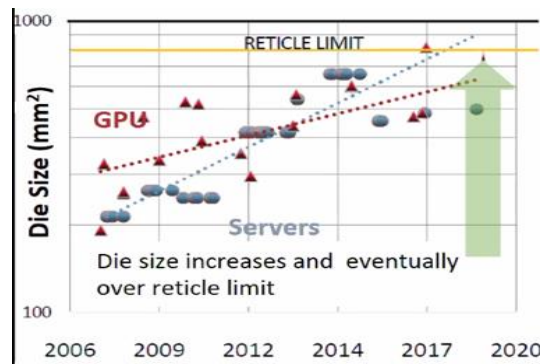
Current Technology Limitations

Investment and design cost per/mm² increasing for advanced nodes



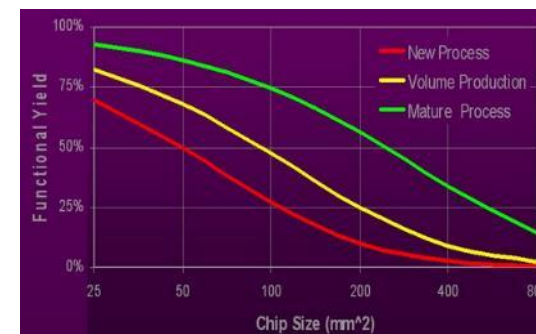
Source: AMD

Size limited by lithography constraints



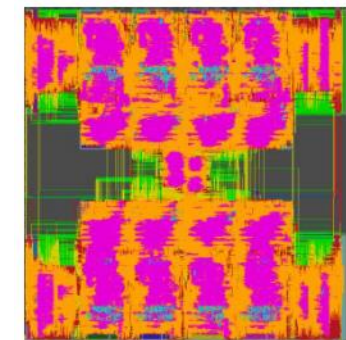
Source: AMD

Usage of larger chips results in lower yields



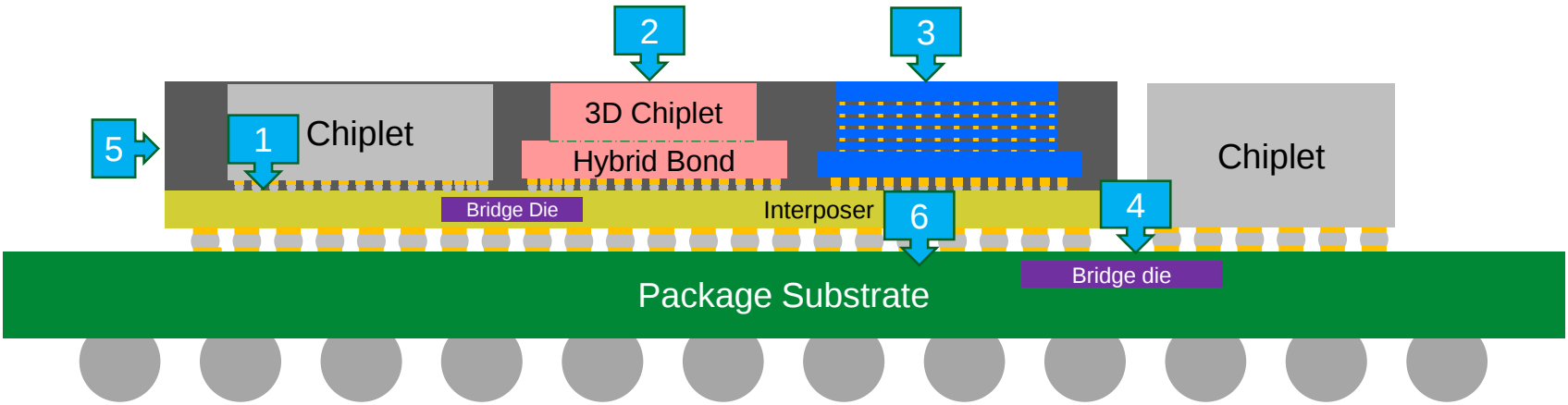
Source: Toshiba

Wire length between sections can become too long

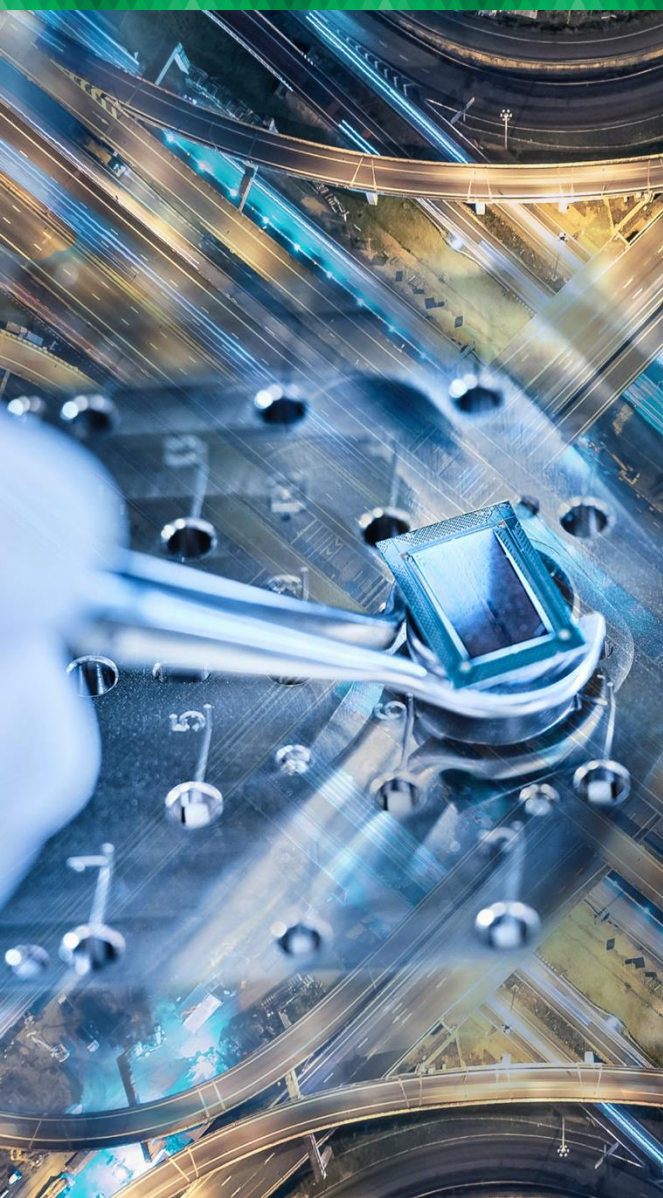


Source: IMEC

Besi Wafer Level Assembly Portfolio Supports Multiple 3D Technologies



1 Chip to Wafer TCB	2 Hybrid Bonding	3 High Bandwidth Memory Stacking	4 Embedded Bridge Die Attach	5 Wafer Level Die Molding	6 HD Interposer to Substrate
TC Next C2W	8800 Chameo Ultra Plus	8800 TC Advanced 8800 Chameo Ultra+	8800 Chameo Ultra	FML	2200 evo



- Overview
- Hybrid Bonding Opportunity
- Q&A

Richard Blickman, CEO

Ruurd Boomsma, CTO