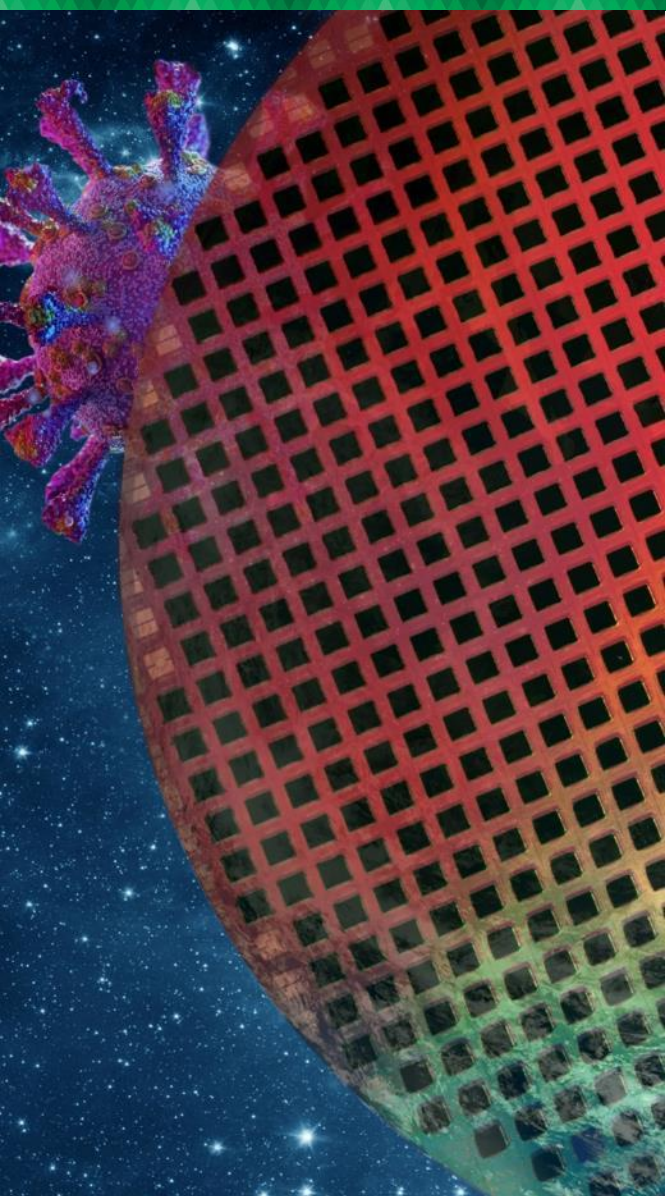


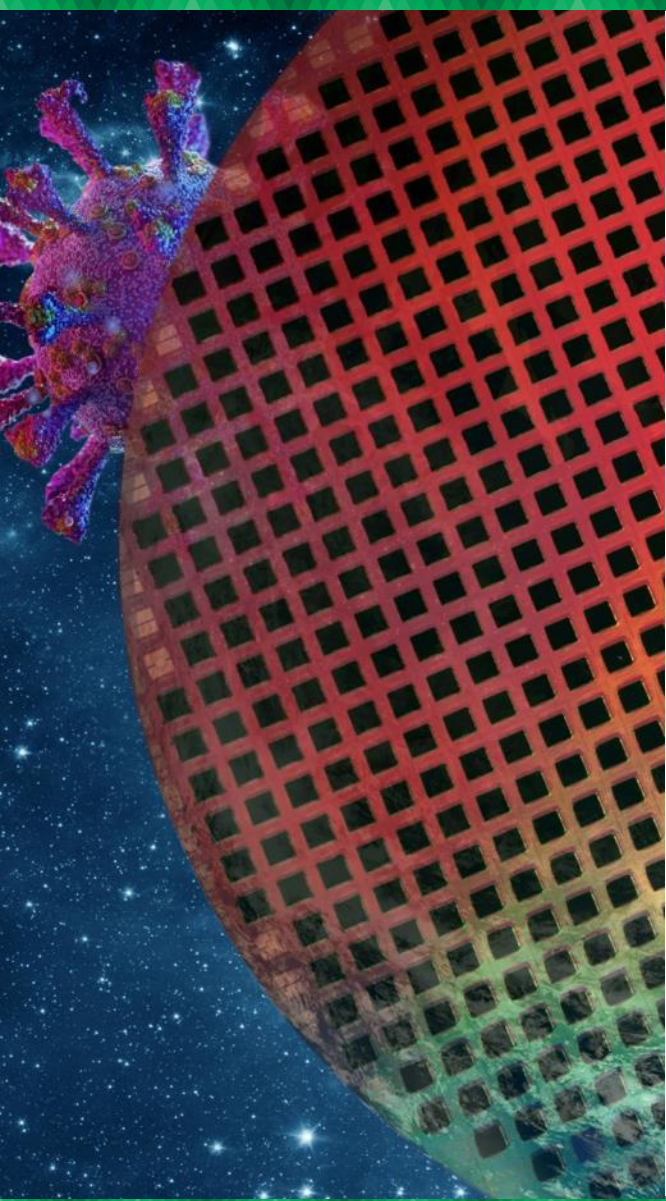


CAPITAL MARKETS DAY PRESENTATION

June 15, 2022

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward-looking statements, which are found in various places throughout the presentation, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward looking statements, although not all forward looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward looking statements. While these forward looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 pandemic and measures taken to contain the outbreak, and the associated adverse impacts on the global economy, financial markets, global supply chains and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; consolidation activity and industry alliances in the semiconductor industry that may result in further increased customer concentration, inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, conflict minerals regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region where we have a substantial portion of our production facilities; our ability to mitigate the dislocations caused by the flood at one of our Malaysian production facilities, potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel, including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers as a result of the COVID-19 pandemic; those additional risk factors set forth in Besi's annual report for the year ended December 31, 2021 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.

I.	Strategic Overview	Richard Blickman
II.	Assembly Market Trends	Ruurd Boomsma
III.	End User Trends	Chris Scanlan
IV.	Mainstream Die Attach	Christoph Scheiring
V.	Wafer Level Assembly	Peter Wiedner
VI.	Packaging/Plating	Jeroen Kleijburg
VII.	Q&A	Besi Team



I. STRATEGIC OVERVIEW

Richard Blickman
CEO



Besi surpassed goals in current cycle

- Revenue and orders of € 749 MM and € 940 MM
- Peer leading net margin 38%, ROI 57%
- Virtually all from Engine 1 advanced packaging portfolio
- Growth from new product innovation, new mobile product cycle and increased market share

Inflection point in assembly market development

- Record \$6.5 billion reached in 2021
- Pandemic accelerated technology adoption and increased investment in AI, 5G, Datacenter and HPC
- Higher advanced packaging capex required to increase chip performance and extend Moore's Law

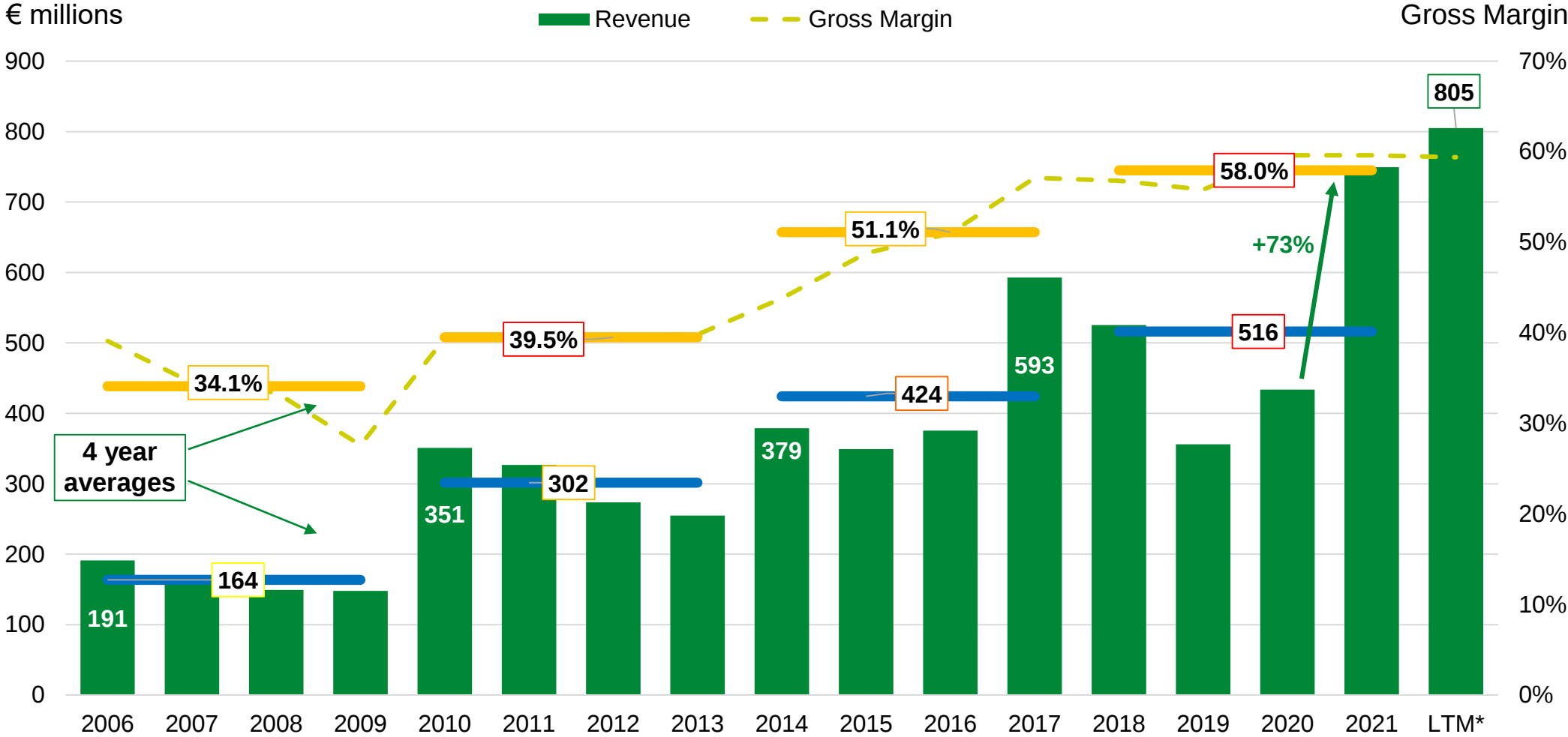
Engine 2 formed to capitalize on wafer level assembly potential

- Hybrid Bonding gateway to new 3D chiplet structures and devices
- Actively pursued by leading front end players
- Facilitates growth for all advanced assembly process technologies
- First mover advantage

Drivers in place to reach \$1 billion +++ model

- Market moving to sweet spot of our core technological competencies
- Besi's addressable market anticipated to grow faster than overall assembly
- Engine 1 can reach € 1 billion next cycle
- Engine 2: +++
 - Hybrid bonding not a question of if, but when, and how large the opportunity
 - Potential market size has increased versus prior forecasts

Structural, Through Cycle, Revenue and Gross Margin Growth Continues



Besi Addressable Market Share Increasing Particularly in Key Die Attach Markets



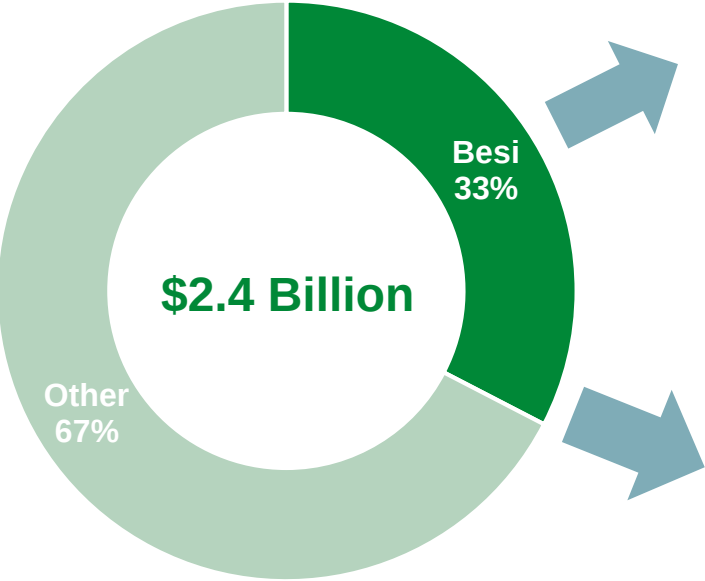
	2016	2017	2018	2019	2020	2021	Δ '21/'20	Δ '21/'16
Assembly Market (\$MM)	3,587	4,648	4,546	3,186	3,843	6,522	+69.7%	+81.8%
Besi Market Share	9.9%	12.7%	11.2%	10.1%	10.7%	11.9%	+1.2pts	+2.0pts
Addressable Market (\$MM)	1,507	1,948	1,859	1,251	1,403	2,374	+69.2%	+57.5%
Besi Market Share	23.7%	30.2%	27.3%	25.8%	29.2%	32.6%	+3.4pts	+8.9pts
Die Attach	30.4%	38.2%	33.2%	30.8%	36.8%	41.9%	+5.1pts	+11.5pts
Packaging & Plating	13.6%	14.7%	17.0%	16.8%	15.3%	15.2%	-0.1pts	+1.6pts
% of Besi Revenue	2016	2017	2018	2019	2020	2021	Δ 1yr	Δ 5yr
Die Attach	75%	82%	76%	76%	82%	82%	-	+7pts
Packaging & Plating	25%	18%	24%	24%	18%	18%	-	-7pts

Source: VLSI June 2022

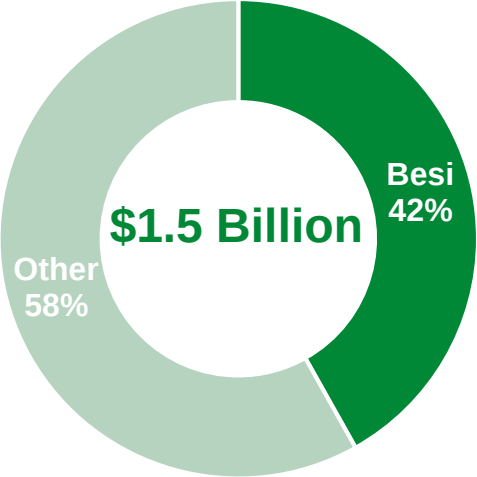
Leader in Addressable Market, Die Attach Market and Advanced Die Placement



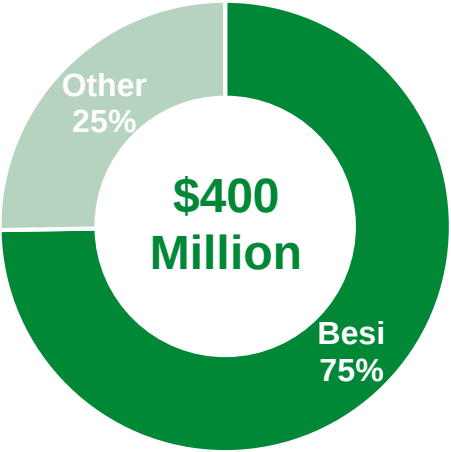
2021 Addressable Market*



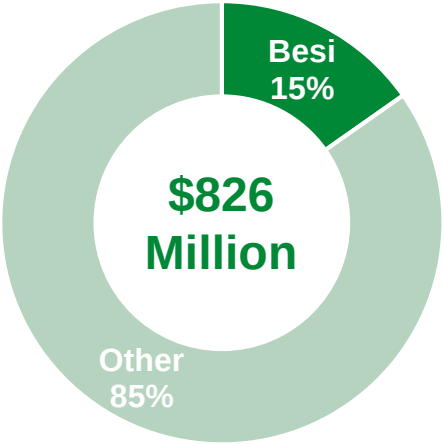
Die Attach
(82% of Revenue)



Advanced Die Placement**



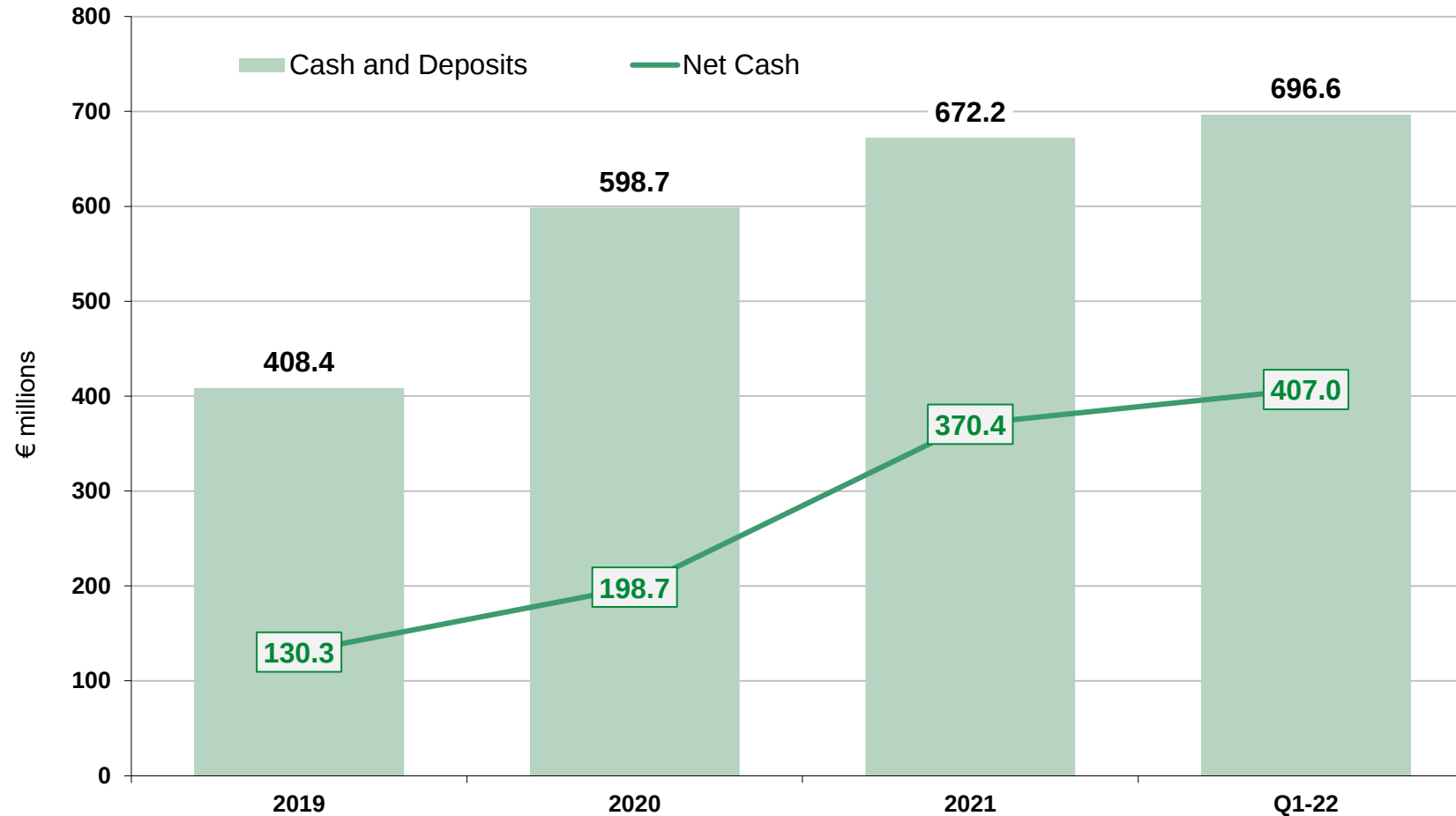
Packaging & Plating
(18% of Revenue)



* Excludes wire bonding, dicing, and other.
** Advanced die placement defined as < 7 micron accuracy per TechInsights

Source: TechInsights, June 2022. Equipment only.

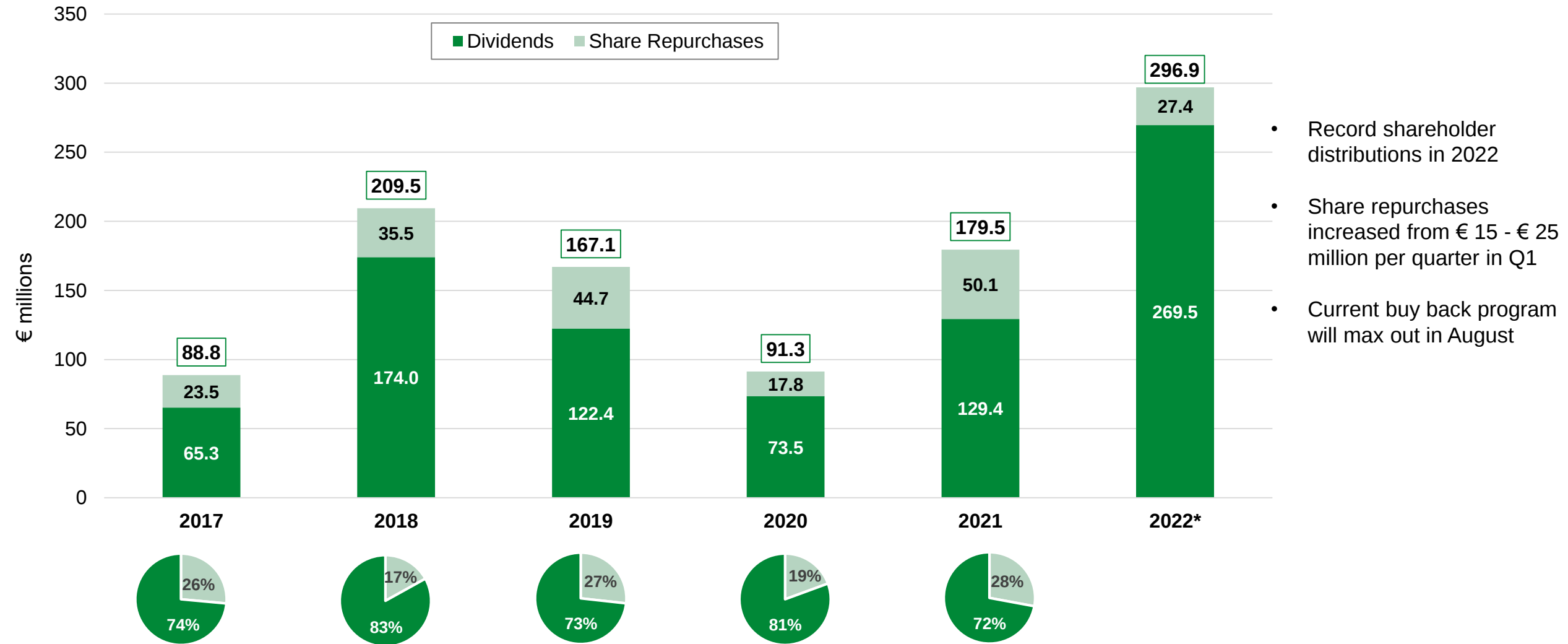
Strong Financial Base to Support Next Phase of Besi's Growth



Besi's liquidity base has expanded:

- Cash grew by 64.6% 2019/2021
- Strong cash flow generation
 - Cash flow from operations was 37% of revenue in 2021
- Attractive financings
 - € 360 million Convertibles outstanding at May 31, 2022
 - Average exercise price of € 68.28/share
 - Blended coupon rate of 1.29%

Commitment to Shareholder Value. €1.2 Billion Returned to Shareholders Since 2011. ~25% of Cumulative Revenue



* Includes dividends and share repurchases through May 31, 2022

Revenue Growth Initiatives

Engine 1

Next gen high end smart phones features & functionality

Advanced logic and memory capex for HPC/data center

Expanded Photonics applications

EV & Autonomous Driving

New assembly solutions for SiC & GaN power devices

Engine 2

Increase engagement top logic and memory players

New 5G, AI, HPC and smart phone applications

New wafer level product introductions

Production/Supply Chain

- Supply chain management top priority
- Ramp HB production. Reduce lead times
- New 125,000 sq ft. Malaysian facility to expand capacity

Development

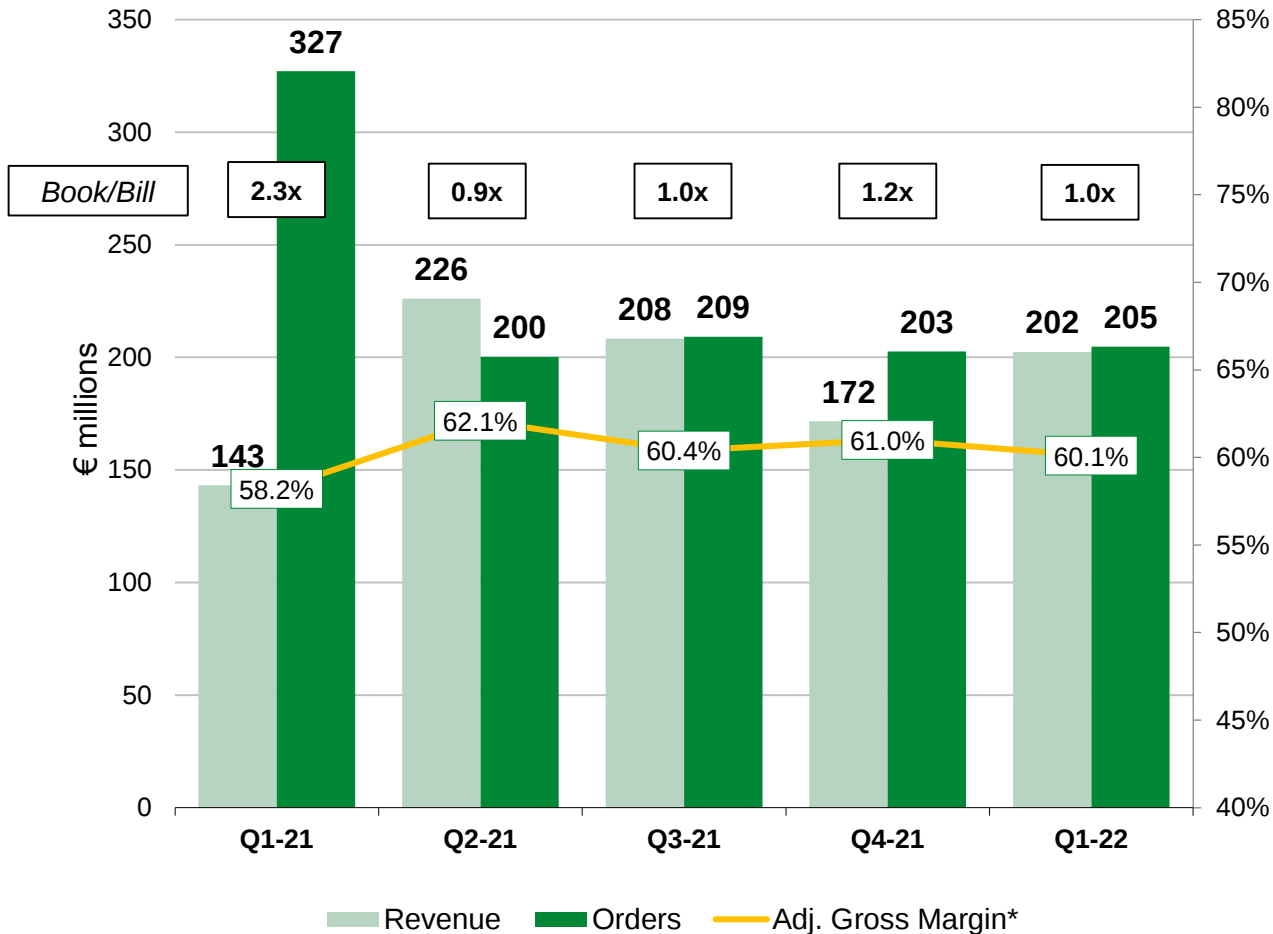
- Next generation HB roadmap:
 - + throughput to 3,000 uph
 - + accuracy to 100 nano
- Roll out new wafer level assembly systems:
 - Embedded Bridge Die Attach
 - TCB C2W

Organization

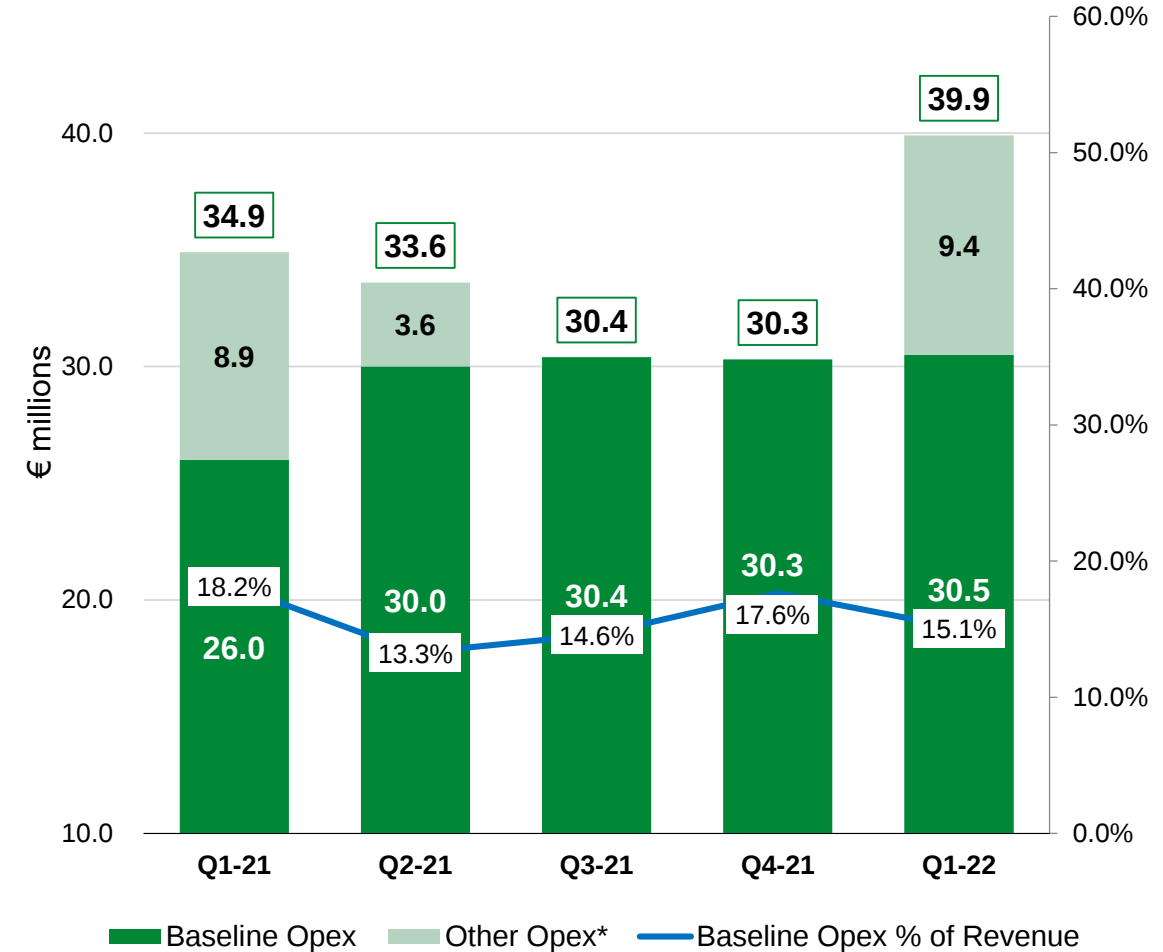
- Implement strategic review initiatives 2021-25

Stable Quarterly Revenue and Gross Margin Development Past 4 Quarters. Initiatives Keep Opex in Check Despite Increased R&D

Revenue, Orders and Gross Margin



Baseline Operating Expenses



* Adjusted to excluded € 7.4 million (4.3 point) inventory charge in Q4-21

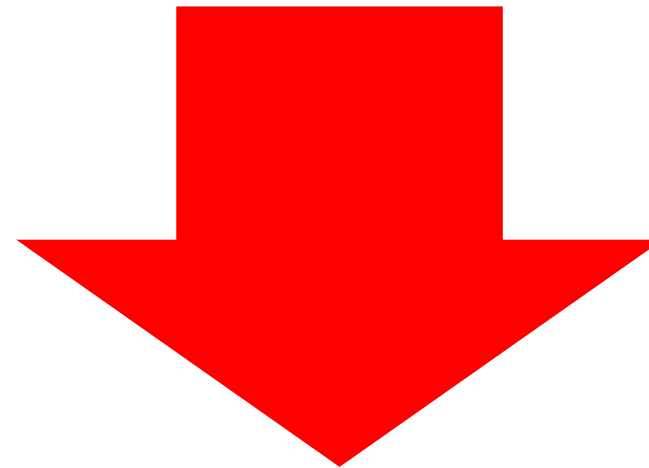


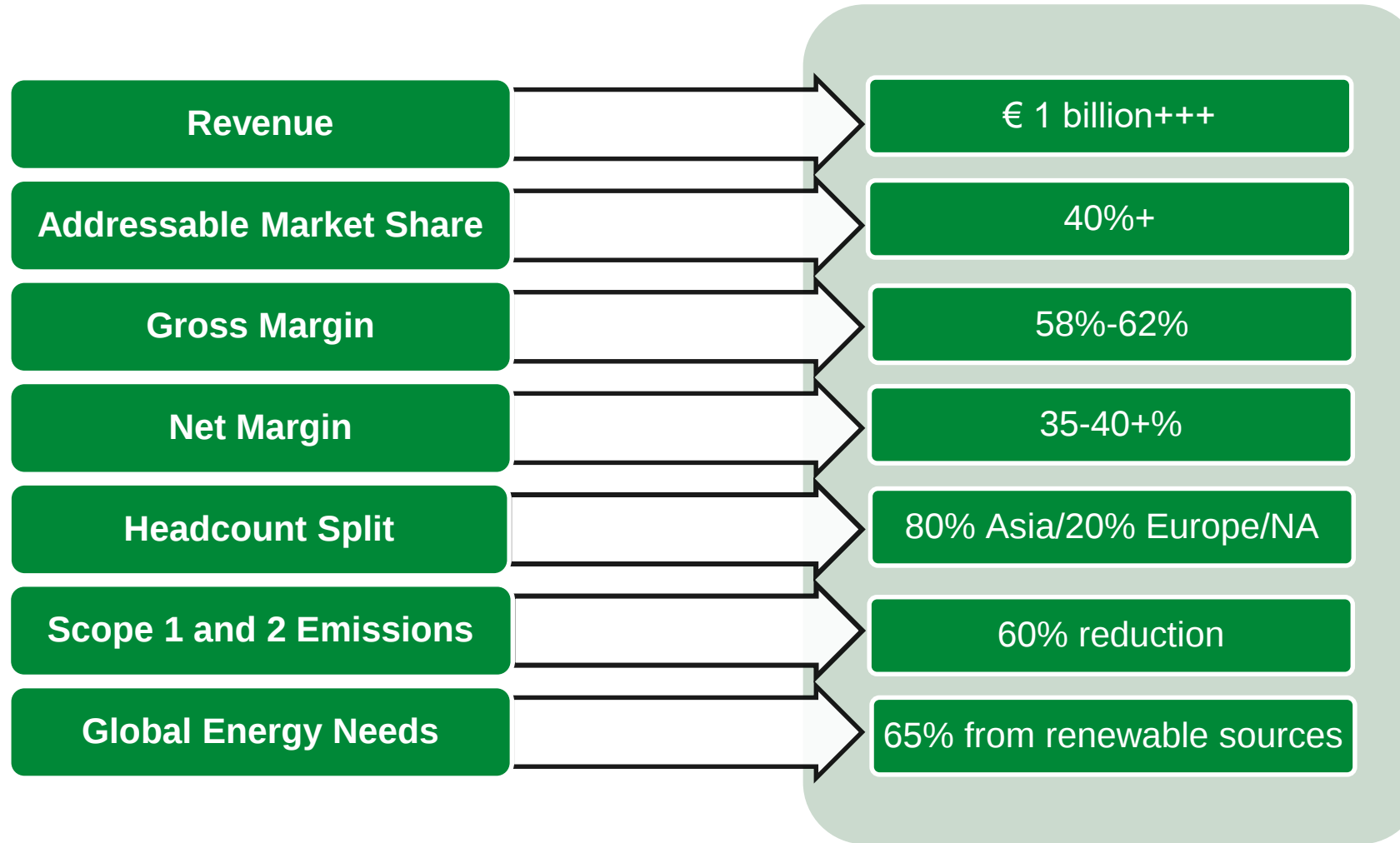
H1-22 growth has continued:

- High Performance Computing
- Automotive
- Capex spending plans of leading semi producers
 - 47 new fabs coming online in next three years
 - Many focus on advanced packaging
 - 2023 High End Smart Phone Cycle???
- Hybrid bonding and wafer level assembly in early stages

Headwinds affect near term orders:

- Decelerating GDP growth post pandemic surge
- Weaker high-end mobile demand
- Weakness in China market:
 - Sufficient capacity built in 2021
 - Rolling COVID lockdowns
- Disruptions to global supply chains
- Geopolitical conflict







II. ASSEMBLY MARKET TRENDS

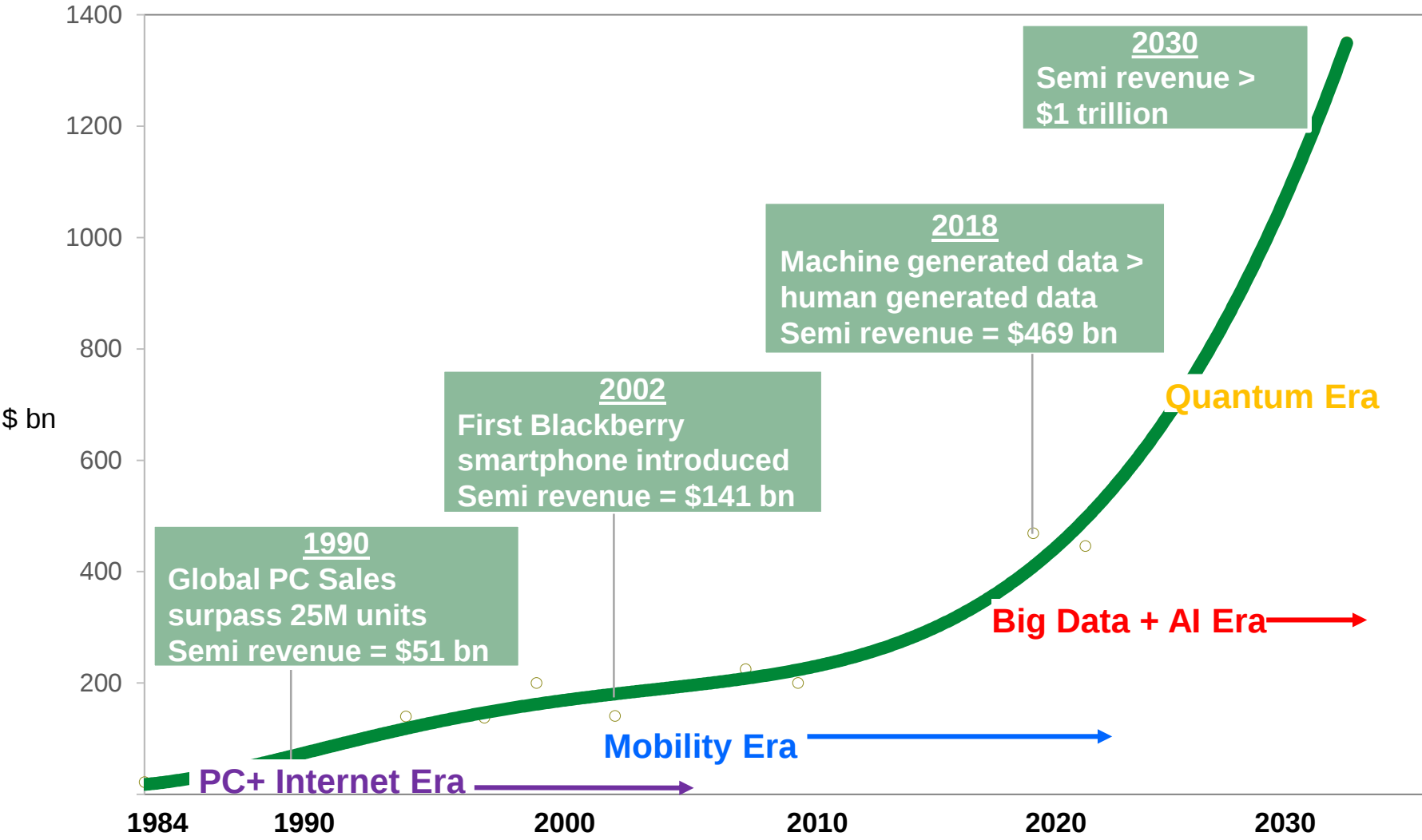
Ruurd Boomsma
Chief Technology Officer



Semiconductor Growth is Accelerating Into Big Data & AI Era



\$500 B sales over past ~50 years → \$1.4T sales over next 10 years



Projected Growth 2020-2030E

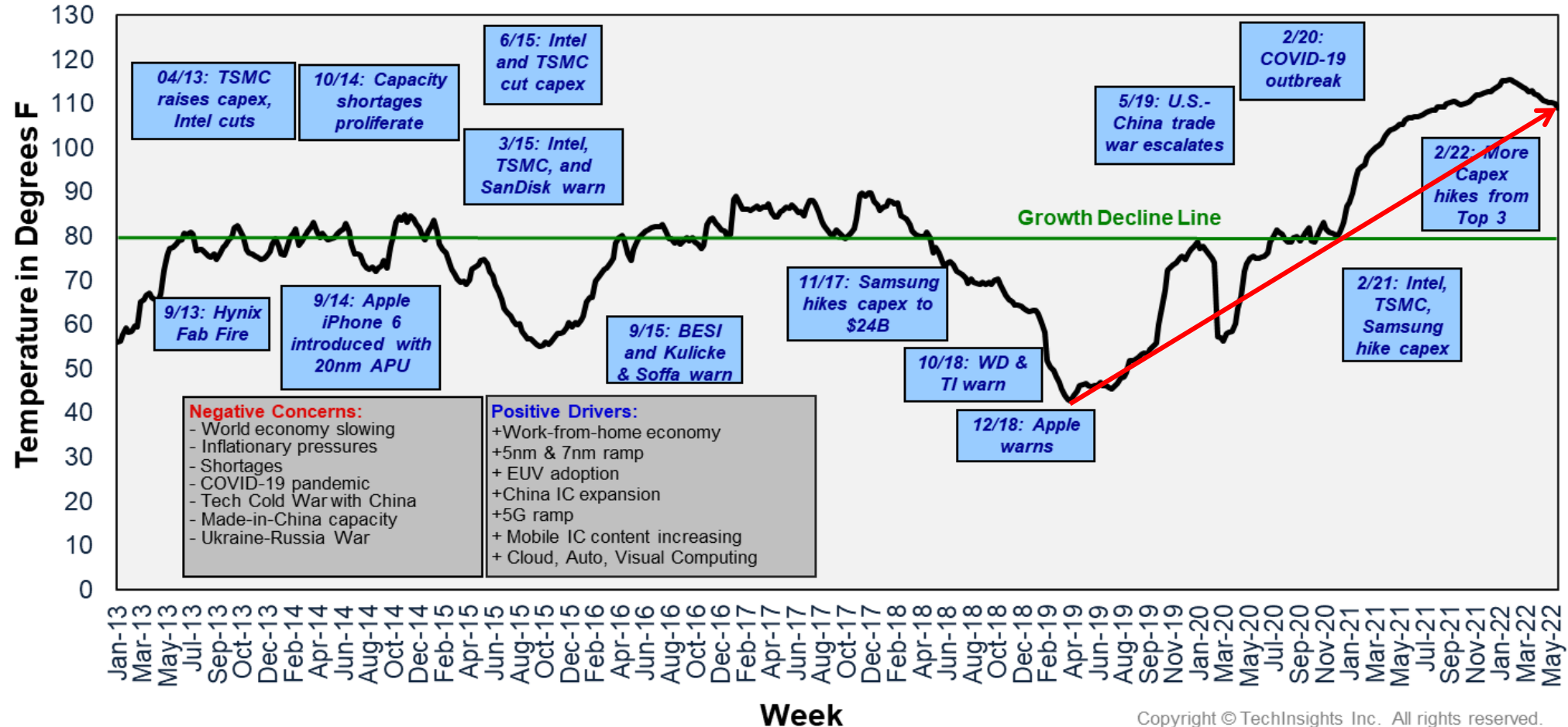
	2020	2030	CAGR
Non-Memory	\$235B	\$678B	11.2%
Memory	\$133B	\$467B	13.4%
Other ICs	\$79B	\$206B	10.1%
Total Semis	\$446B	\$1,351B	11.7%

Data source: Semi 2022

Industry Upturn Levelling Off in H1-22

TECHINSIGHTS' GLOBAL CHIP MAKING CLIMATE TREND INDEX

(Average of Regional Order Activity Patterns in Chip Equipment)



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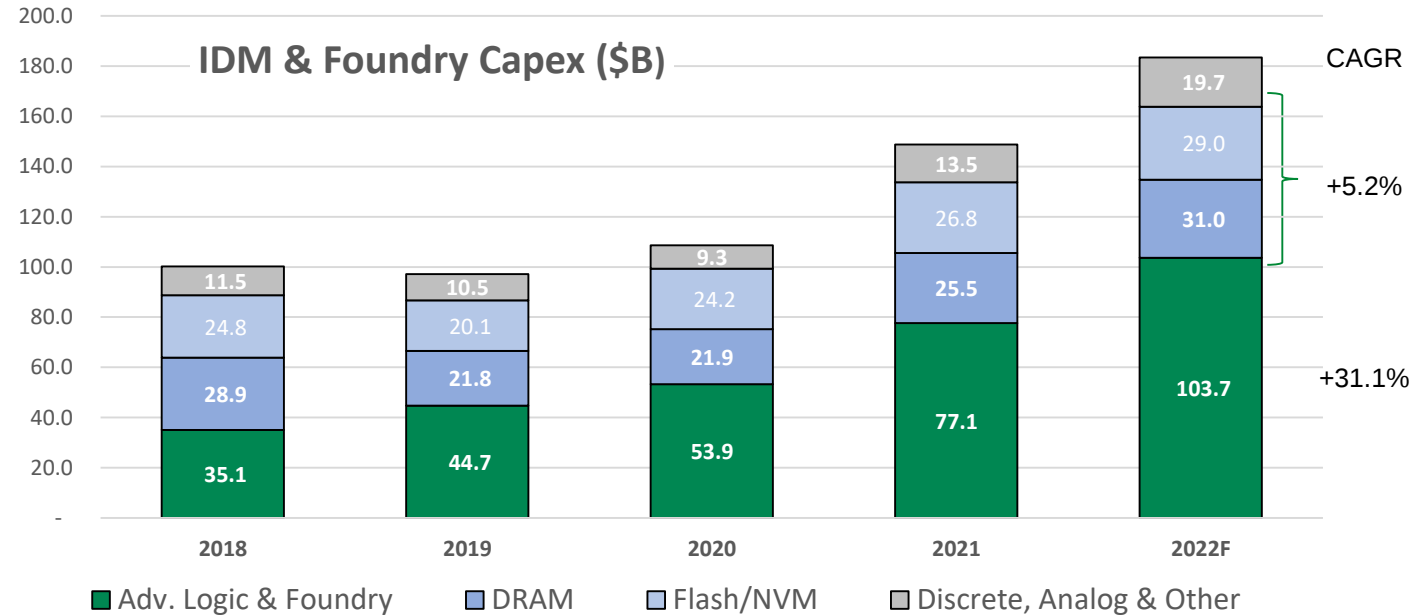
Source: Tech Insights, June 2022

Semi Capex Expected to Increase 23% in 2022 to Reach \$183.4 Billion



TOP IDM & FOUNDRY CAPEX SPENDERS (Capital expenditures by company, \$B, ranked by 2022 Forecast)					
	2018	2019	2020	2021	2022F
TSMC	10.5	14.9	17.2	30.0	44.0
Samsung	21.6	19.3	28.1	38.0	35.9
Intel	15.2	16.2	14.3	18.7	27.0
SK hynix	14.6	12.0	8.4	10.9	13.9
Micron Technology	8.8	8.6	8.8	10.2	11.3
KIOXIA/WD	3.2	2.9	3.5	5.4	4.1
SMIC	1.8	2.0	5.7	4.5	5.0
STMicroelectronics	1.3	1.2	1.3	1.8	3.5
XMC/YMTC	2.4	2.1	2.9	3.1	3.4
Sony	1.4	2.3	2.4	2.7	3.2
UMC	0.7	0.6	1.0	1.8	3.6
GLOBALFOUNDRIES	1.2	0.6	0.6	1.0	3.0
Innotron	1.3	1.4	2.5	2.8	2.7
Huahong Group	2.2	2.0	2.2	1.9	2.2
Infineon	1.4	1.3	1.1	1.6	1.9
Nexchip	0.8	0.6	0.8	0.8	0.8
Others	12.0	9.3	8.0	13.3	18.1
Total	100.2	97.1	108.6	148.7	183.4
<i>y-o-y growth</i>	<i>8%</i>	<i>-3%</i>	<i>12%</i>	<i>37%</i>	<i>23%</i>

Top 3 (% of Total)	52%	55%	58%	58%
Top 5 (% of Total)	73%	71%	73%	72%



2022 Semi capex growth +23% by VLSI

- 64% of estimated increase represented by TSMC and Intel
- Powered by Advanced Logic and Foundry (+35% vs. 2021)

Growth in Advanced Logic and Foundry has significantly exceeded memory spending in recent years

- CAGR of 31.1% 2018-2022 vs. DRAM/Flash/NVM CAGR 5.2%
 - Represents 57% of total WFE spending in 2022

Industry consolidating: top 5 producers now represent 72%

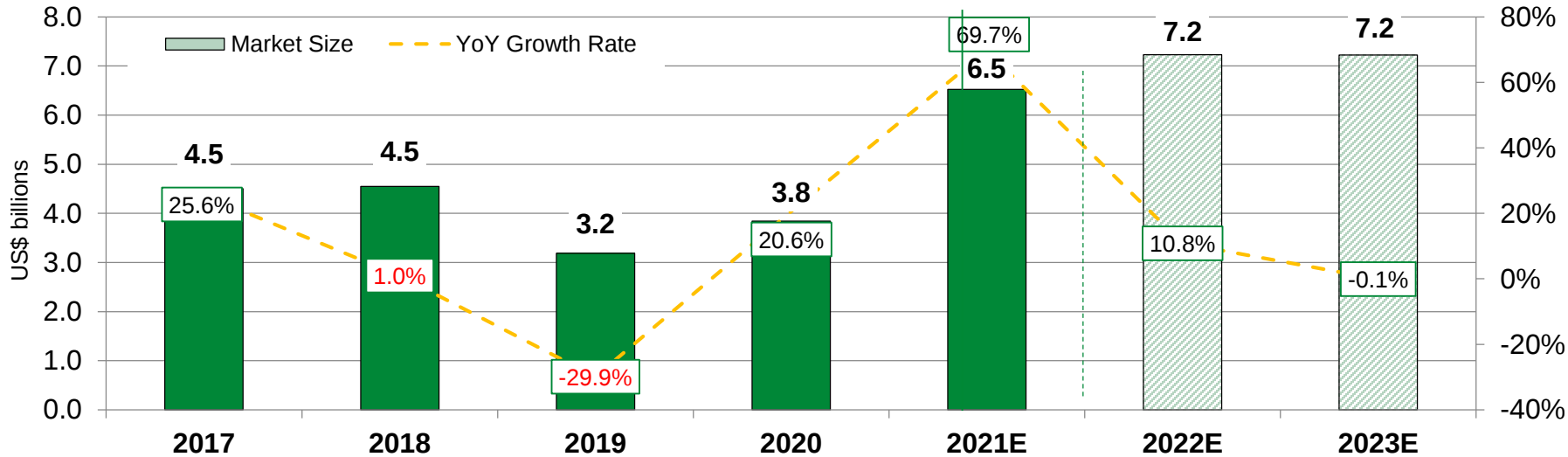
Capex Spending Plans by Leading Producers to Increase in 2022

\$98.4 Billion Direct and \$164.4 Billion Indirect Spending/Annum Planned

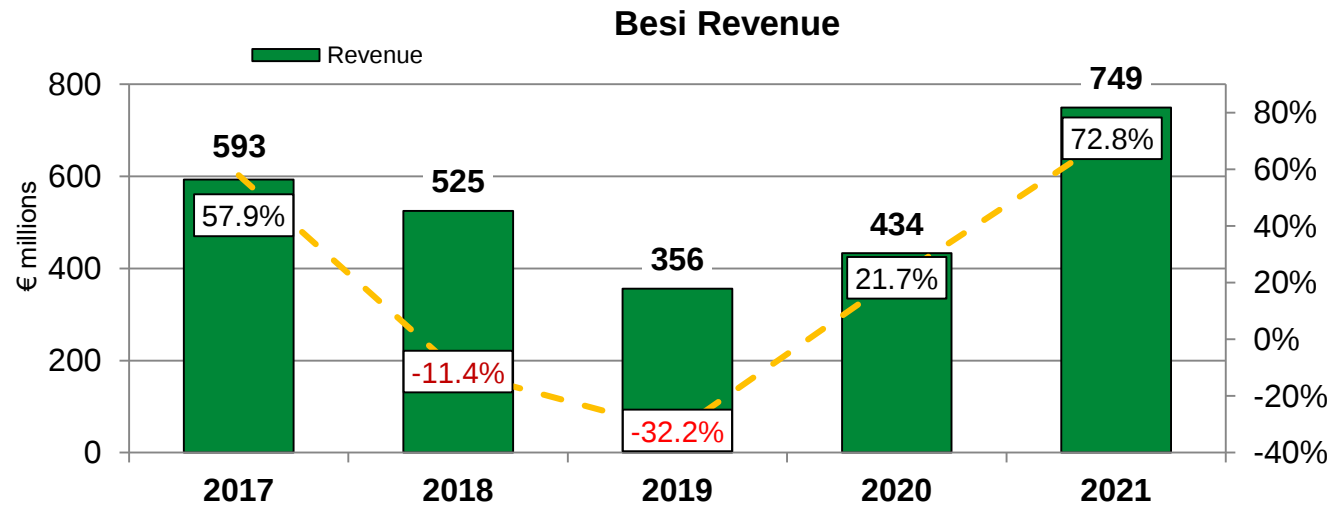


TechInsights June 2022	Date	Amount \$	Timing	\$ p.a.	Location	Purpose
Direct Investments						
TSMC	Mar 2021	100.0B	3 years (2023)	33.0B	Taiwan/AZ	Advanced packing capacity and R&D
TSMC	May 2021	12.0B	3 years (2024)	2.4B	AZ	New 5nm fab
Intel	Mar 2021	20.0B	3 years (2024)	6.7B	AZ	2 new fabs <7nm
Intel	May 2021	3.5B	3-4 years (2025)	1.0B	NM	Fab upgrade Adv. Packaging
Intel	Jan 2022	20.0B	3 years (2025)	6.7B	OH	2 new fabs leading edge
GLOBALFOUNDRIES	June 2021	6.0B	3 years (2024)	2.0B	Singapore	Expansions/adding capacity
Texas Instruments	Feb 2022	14.0B	4 years (2025)	3.5B	USA	Add capacity
Samsung	Aug 2021	205.0B	9 Years (2030)	22.8B	KO/CN/US	Foundry <3nm and Adv. Memory
SK Hynix	May 2021	203.0B	10 Years (2030)	20.3B	KO/CN	Adv. Memory and capacity expansion
Indirect Investments						
Apple	Apr 2021	430.0B	5 years (2026)	86.0B	USA	Next-gen silicon, 5G innovation, data centers
Intel	Mar 2022	€ 80.0B	10 years (2032)	€ 8.0 B	EU	European Union/Semi Capacity
USA	May 2021	52.0B	5 years (2026)	10.4B	USA	Semi capacity and R&D
EU	Dec 2020	€ 30.0B	5 years (2025)	€ 6.0B	EU	Semi capacity and R&D. ESG
EU	Feb 2022	€ 15.0B	8 years (2030)	€ 1.9B	EU	European Chips Act
Korea	May 2021	450.0B	10 years (2032)	45.0B	KO	Semi manufacturing incentives
Japan (Sony/TSMC)	May 2021	16.0B	3 years (2024E)	5.3B	JP	<20nm fab

Assembly Equipment Forecast



Source: Tech Insights, June 2022. Assembly equipment revenue excludes hybrid bonding contribution and service revenue.



+69.7% growth now estimated for 2021

- Upsized from 55.6% last quarter
- Market reached record \$ 6.5 billion

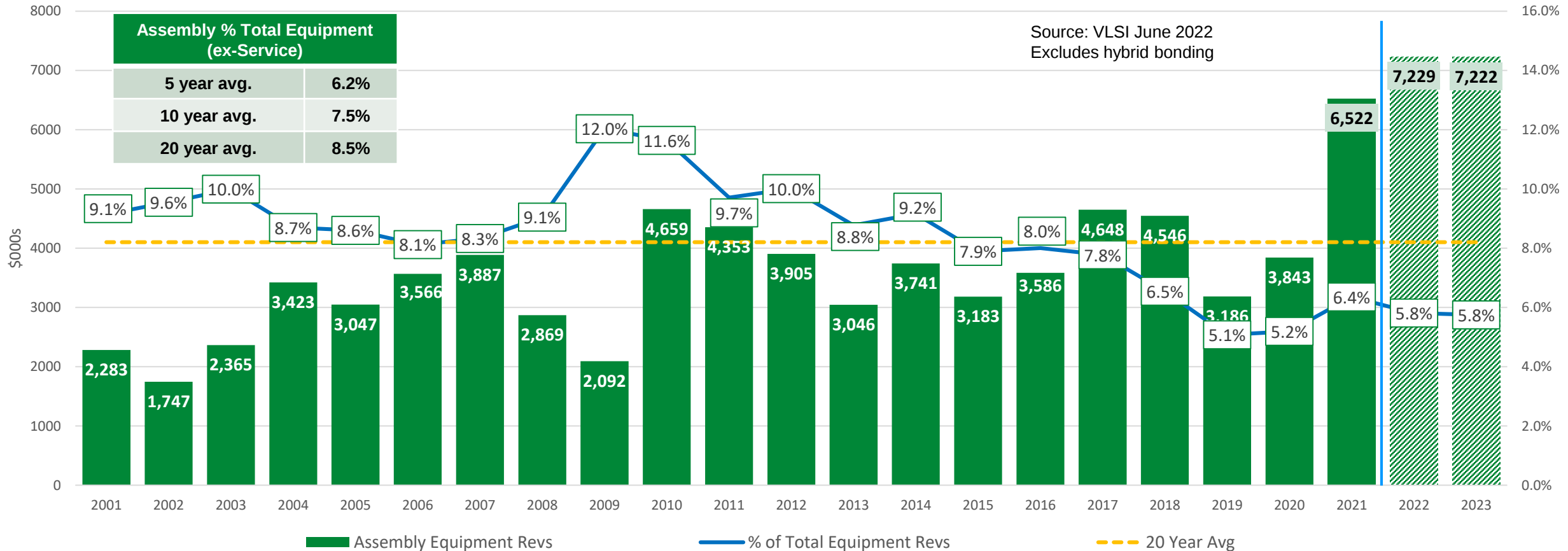
Tech Insights expects market to reach \$ 7.2 billion in 2022 (+10.8%)

- Excluding hybrid bonding and spares/service revenue

Strong secular market fundamentals:

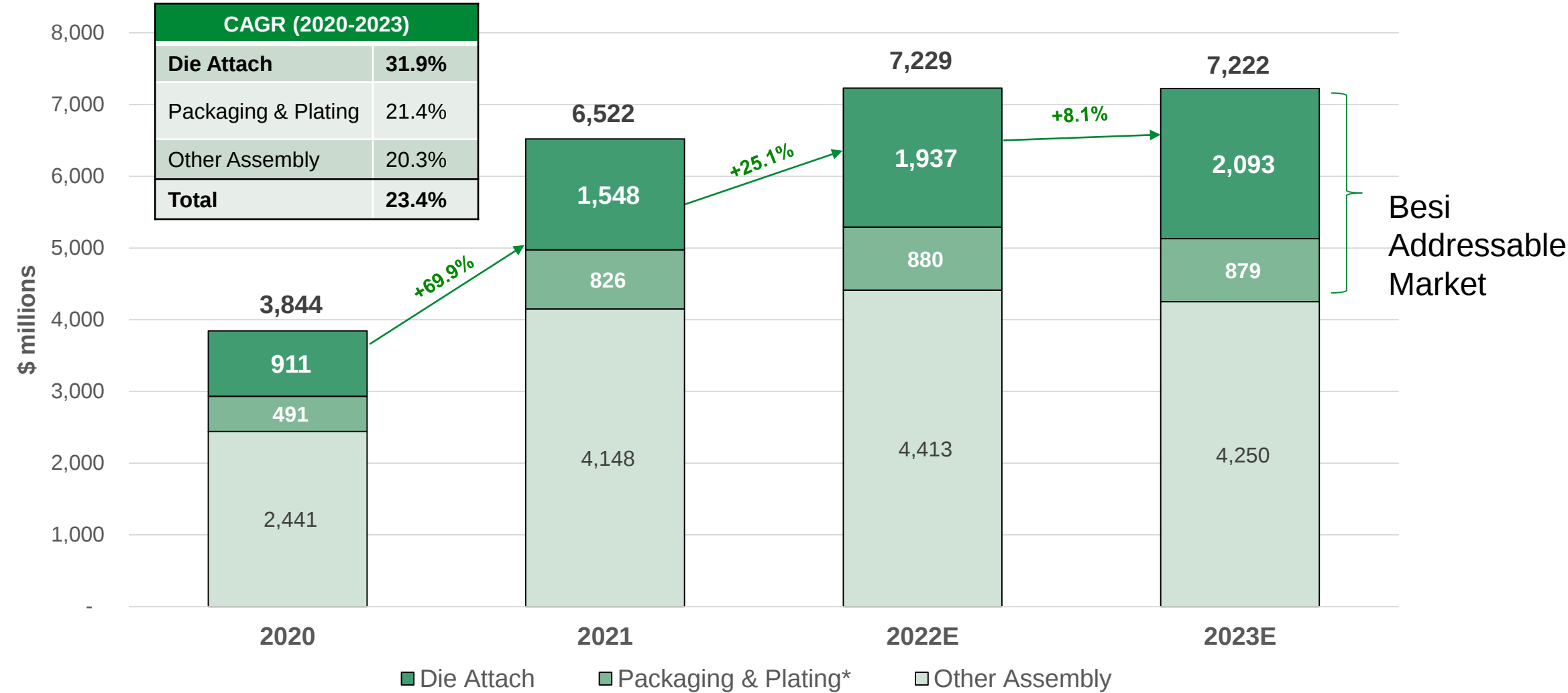
- 5G, Datacenter, AI and HPC primary drivers
- Investment in new process technologies: hybrid bonding/CSP

Assembly Capital Intensity Rebounded in 2021

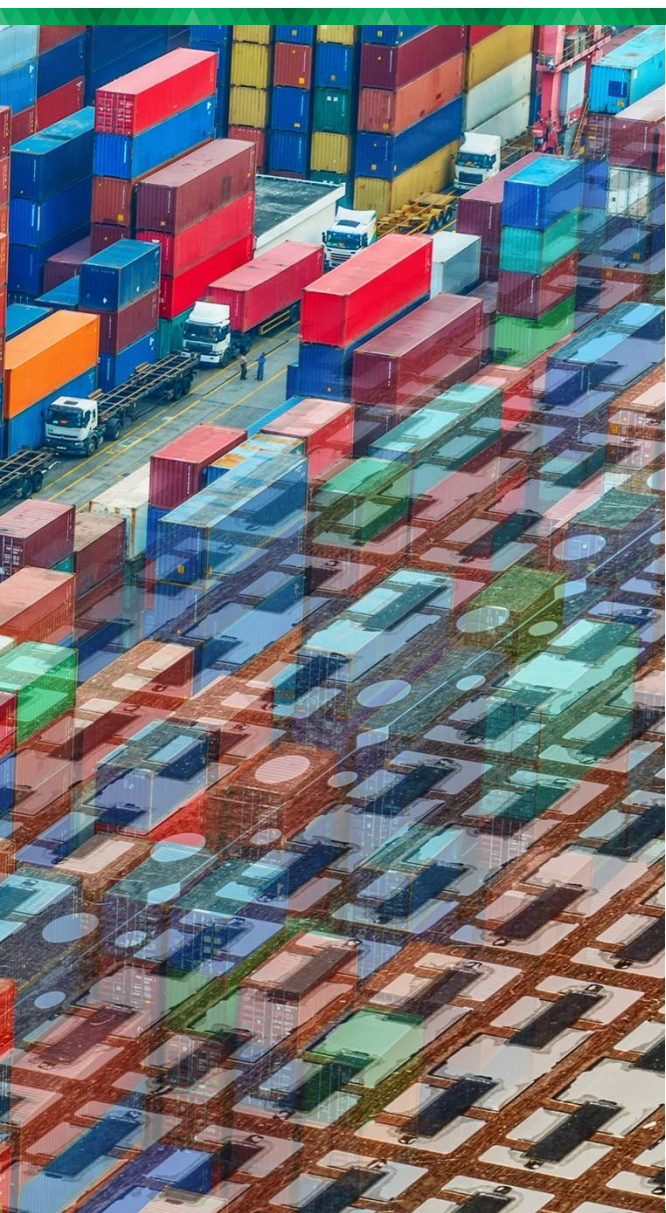


- Traditional component assembly investment has lagged WFE in recent years
- Reached trough in 2019/2020
- Capital intensity rebounded in 2021
 - Investment in <10nm devices could drive % higher in next 5 years

Growth Expected to Favor Besi's Product Portfolio, Particularly Die Attach



Source: Tech Insights, June 2022. Addressable market revenue excludes hybrid bonding contribution.
* Packaging & Plating includes only Besi's addressable segments. Non-addressable reported in other assembly market.



III. END USER TRENDS

Chris Scanlan
SVP Technology



Besi Principal End User Markets



<u>Mobile Internet (39%)</u> 5G Ramp Underway	<u>Computing (21%)</u> Digital Society Accelerating	<u>Automotive (13%)</u> Electrification & Automation	<u>Industrial/Other (10%)</u> Energy Efficient/Green

ALL CONNECTED IN MANY DIFFERENT WAYS



Percentages based on Besi’s 2021 estimated revenue per end market application. Spares/service revenue was ~17% of 2021 revenue.

Key End User Application Drivers

Projected growth requires more semiconductor content with new, highly integrated packaging solutions

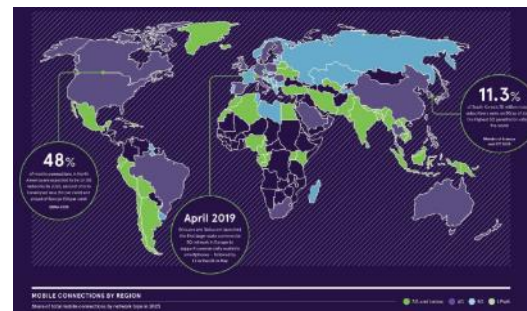
Data Center



Web 3



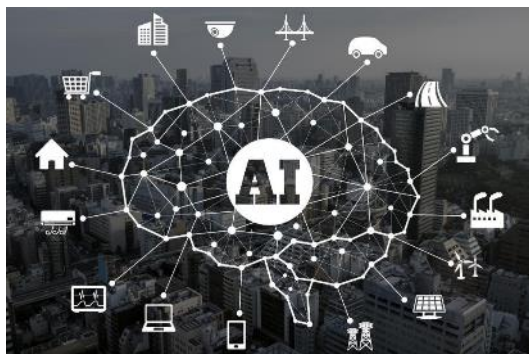
5G Rollout



EVs



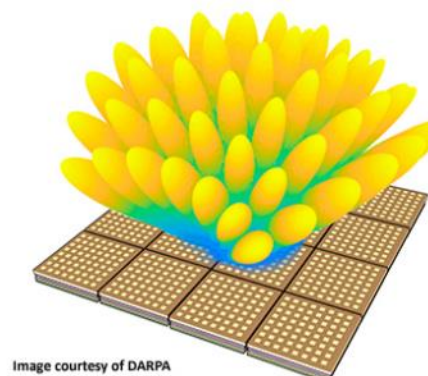
Artificial Intelligence



Pervasive Connectivity



mmWave → 6G



Autonomous Driving

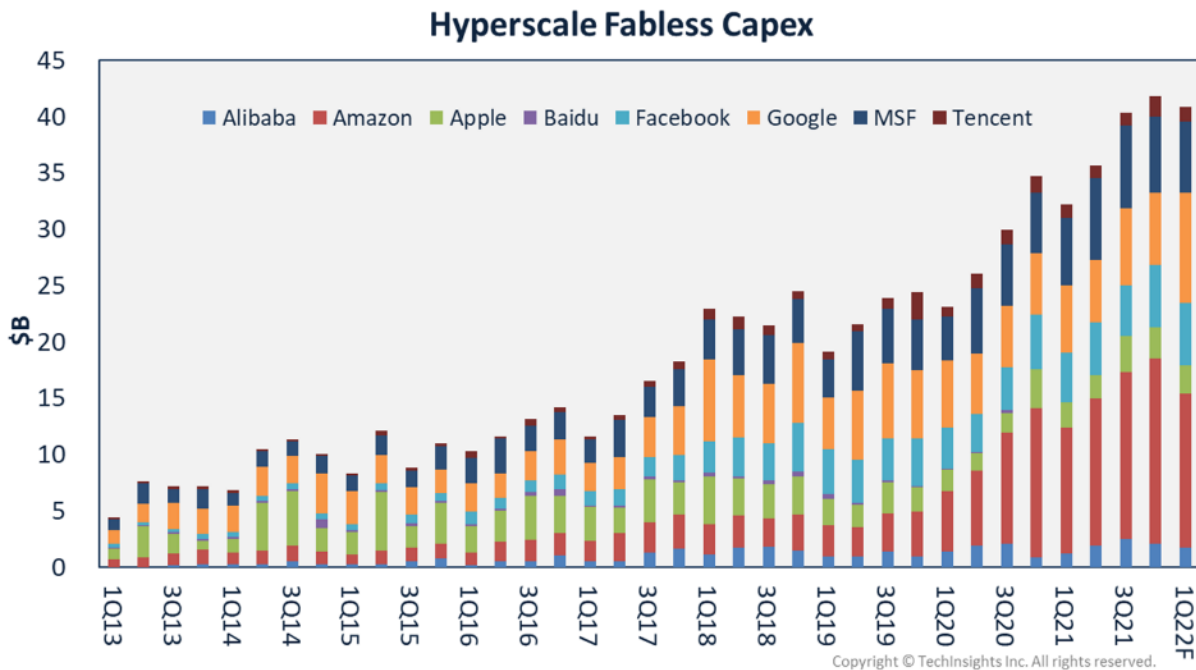


Computing is One of Besi's Fastest Growing End Markets



Growth of cloud infrastructure investment continues

- Driven by exponential growth of information created, captured, copied and consumed



Compute fastest growing foundry segment through 2025

- Compute overtook mobile segment in 2021
- Foundry growth now led by HPC

Foundry Revenue Forecast and Mix% by Industry



High performance computing is driving rapid innovation in chiplet assembly technologies

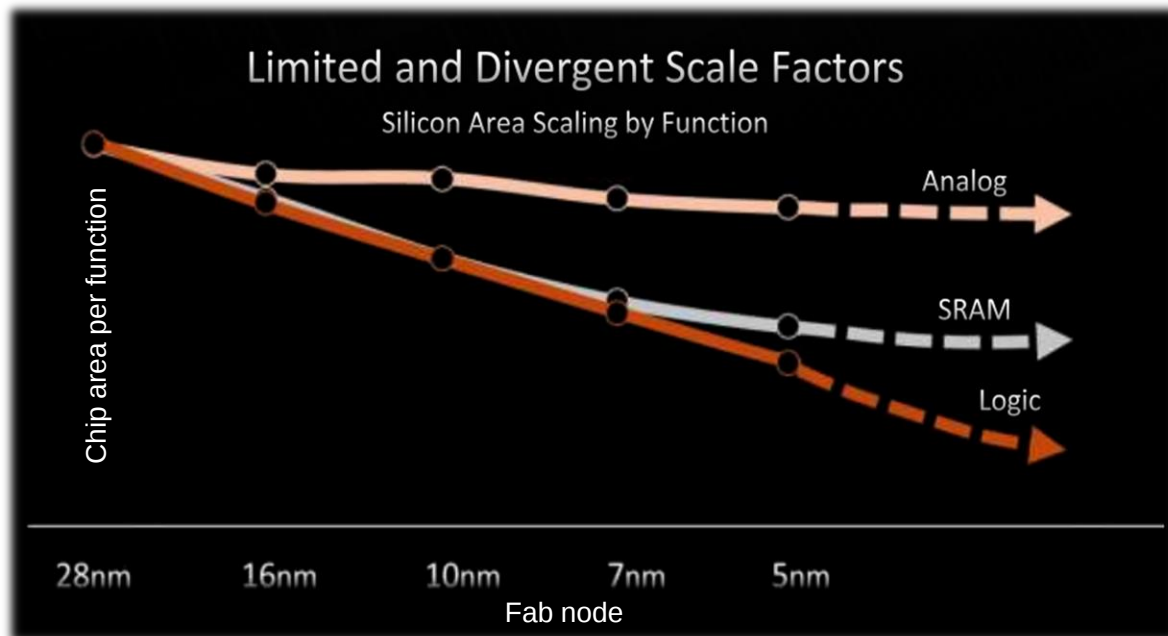
Slowing of Moore's Law Drives Adoption of Chiplet Architectures and New Assembly Solutions

Problem

- Moore's Law is slowing
- Some functions don't shrink as node sizes reduce
- Die sizes are increasing beyond reticle limit

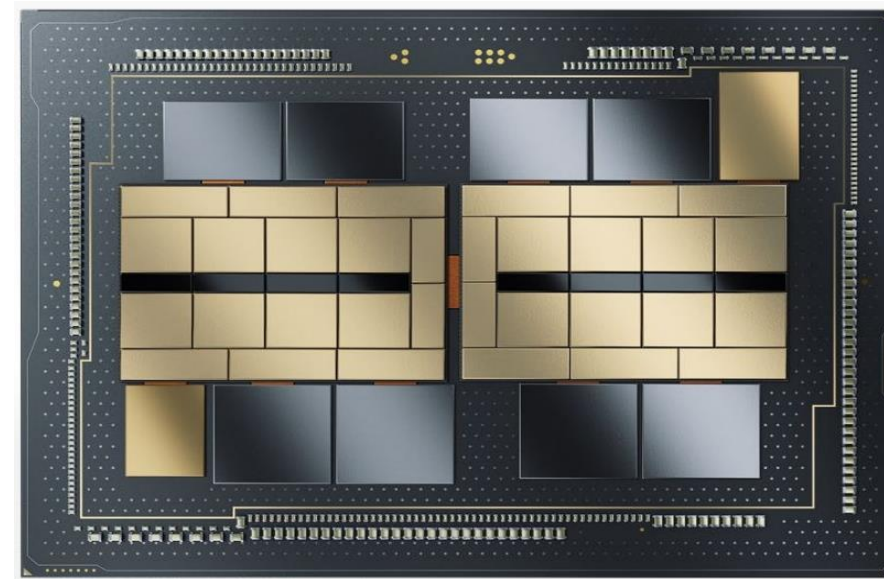
Solution

- Split the SoC into multiple, smaller **chiplets**
- Optimize scale per function
- Connect chiplets within the package utilizing advanced **chip-to-wafer die attach**



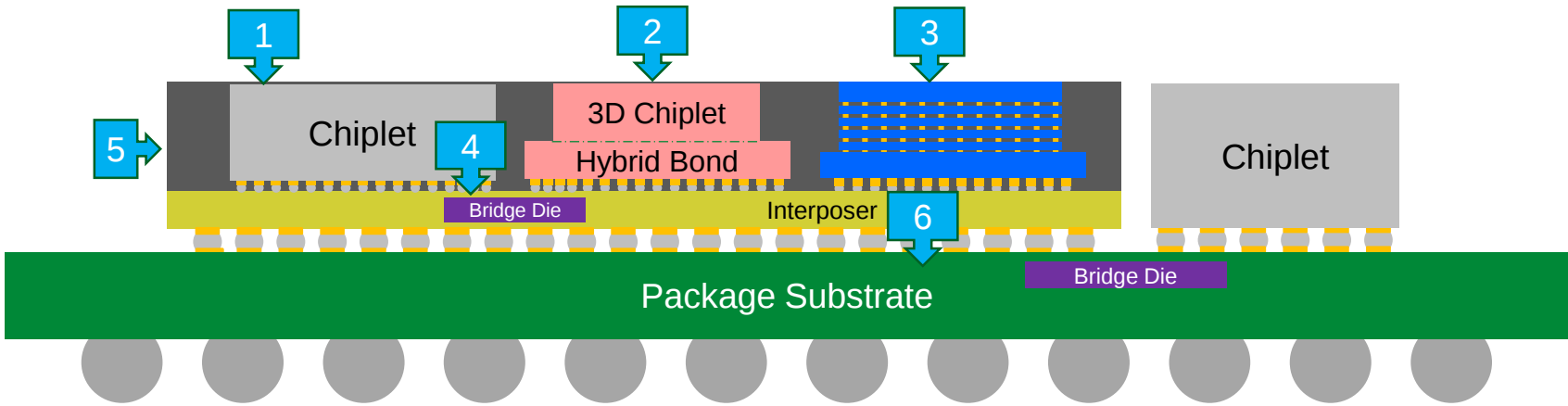
Source: AMD

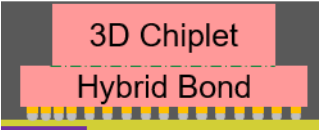
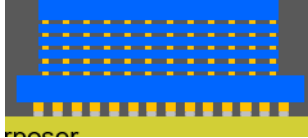
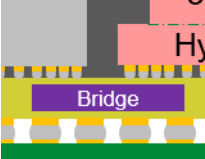
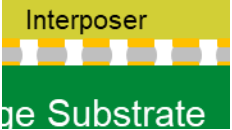
Intel's Ponte Vecchio: 47 Chiplets in One Package



Source: Intel

New 3D Chiplet Structures Use Variety of Advanced Assembly Processes



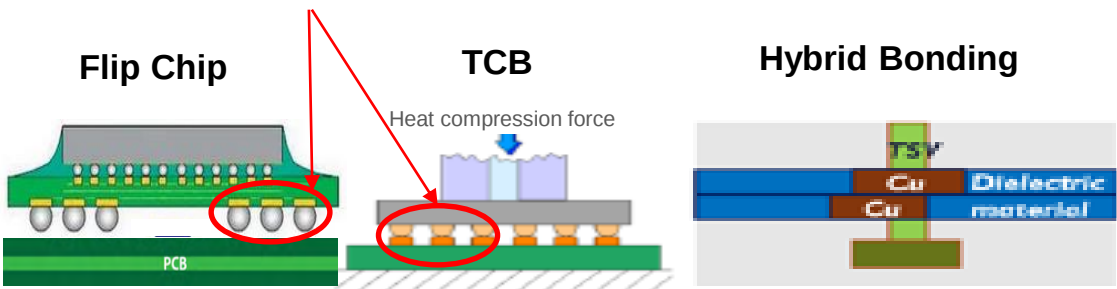
1	2	3	4	5	6
Chip to Wafer TCB	Hybrid Bonding	High Bandwidth Memory Stacking	Embedded Bridge Die Attach	Wafer Level Die Molding	HD Interposer to Substrate
					
TC Next C2W	8800 Chameo Ultra Plus	8800 TC Advanced 8800 Chameo Ultra+	8800 Chameo Ultra	FML	2200 evo

Why is Hybrid Bonding Important?

Direct Cu-Cu Interconnect

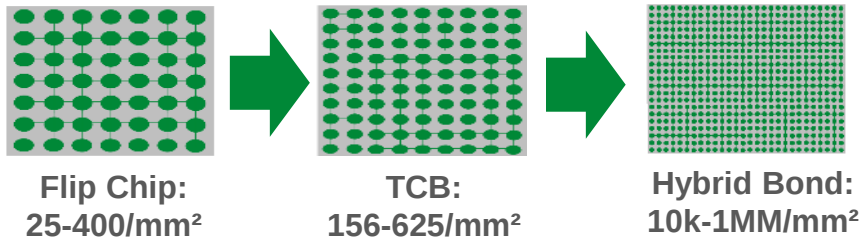
Eliminates need for interposer & solder balls

Results in smaller, thinner form factor to design more complex devices



Ultra-High Bandwidth & Speed

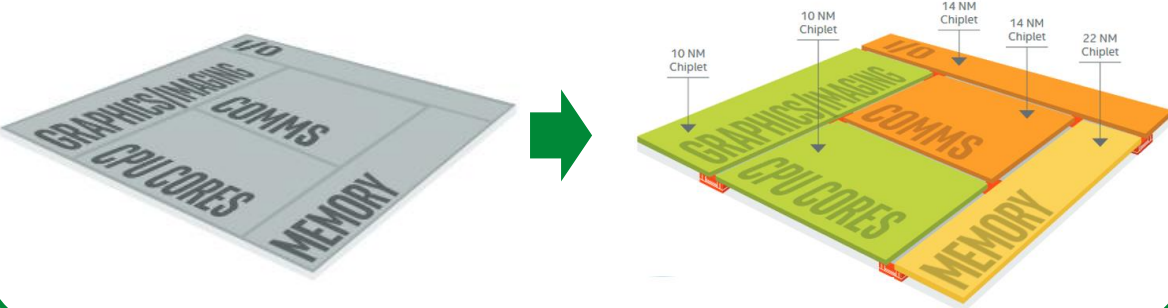
Contact density increased by factor of 1000x by eliminating solder balls, reducing distance between contacts & increasing speed & data transfer



Current design achieves 122 nano placement accuracy at 2,000 uph

Design Flexibility

Hybrid bonding facilitates development of new 3D chiplet architectures and increased features/functionality in smaller form factor



Lower Cost of Ownership

Lower Cost of Ownership

- Performance and functionality increased
- Fewer chips required
- Materials cost lower
- Cost per contact lower
- Lower heat dissipation
- Energy consumption lower

Energy Efficiency

Process	Flip Chip	TCB	Hybrid Bonding
Energy/Bit	0.5pJ/bit	0.1pJ/bit	<.05pJ/bit

Smaller devices draw less electrical power

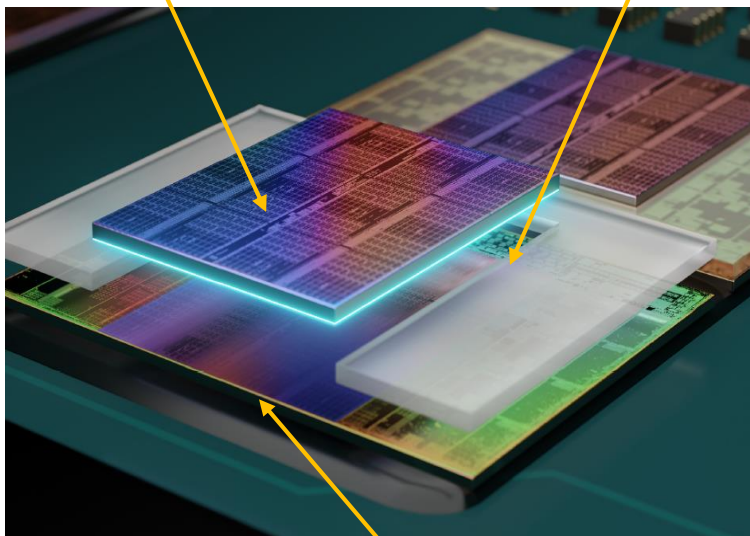
AMD Shipping First CPUs Using Hybrid Bonding

Ryzen CCD with 3D V-Cache

- Additional 64 MB SRAM stacked atop Ryzen chiplets using hybrid bonding
- Realized 3X increase in L3 cache

SRAM die hybrid bond
to back of CCD chip

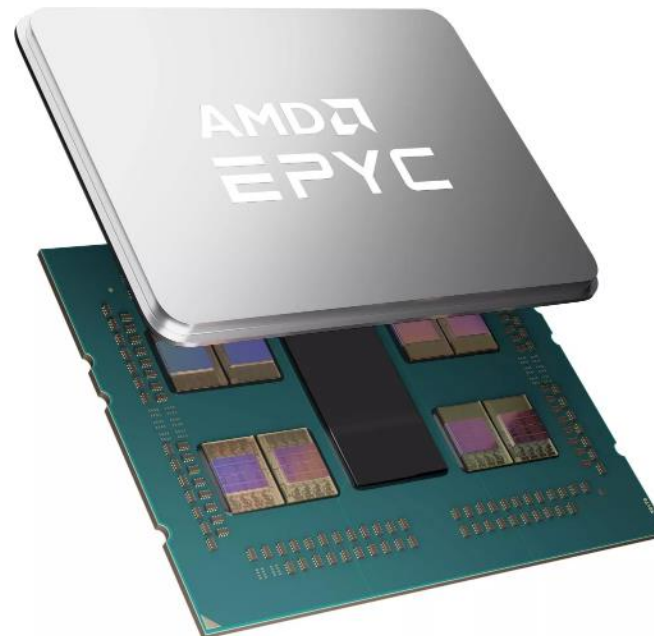
2 structural Si die
hybrid bonded to CPU



Ryzen CCD chip with TSVs attached to package substrate using standard flip-chip process

EPYC Milan X

- First product with 3D V-Cache
- 8 Ryzen CCD chiplet assemblies
- One I/O chiplet on 14nm node



Ryzen™ 7 5800X3D

- Gaming processor with a single Ryzen CCD chiplet + custom I/O chiplet



New Chiplet Architectures Increase Process Steps/Capital Intensity

2017

2019

2022

1st Gen EPYC

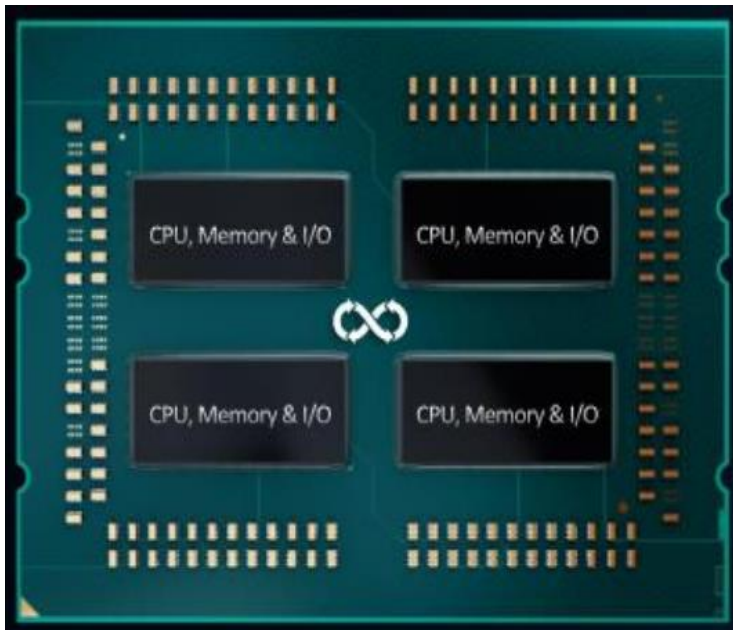
2nd Gen EPYC

3rd Gen EPYC

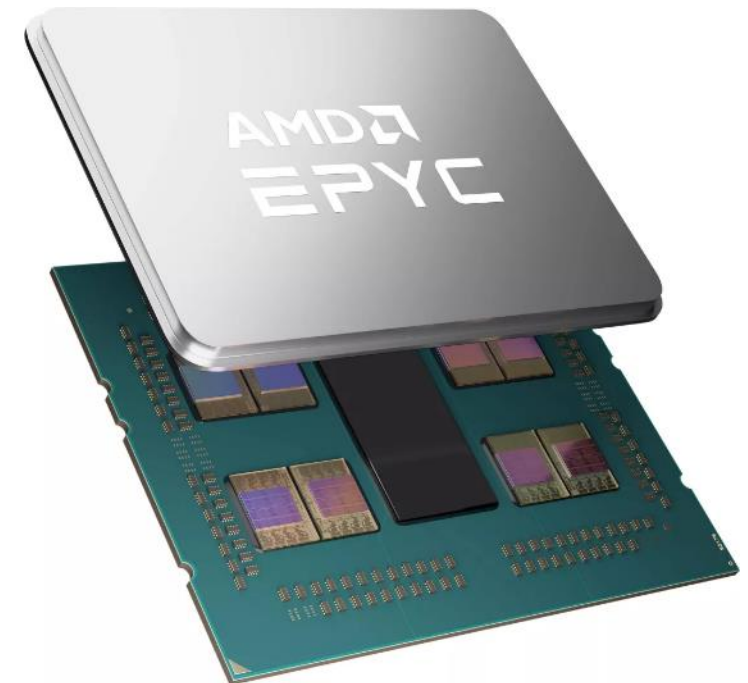
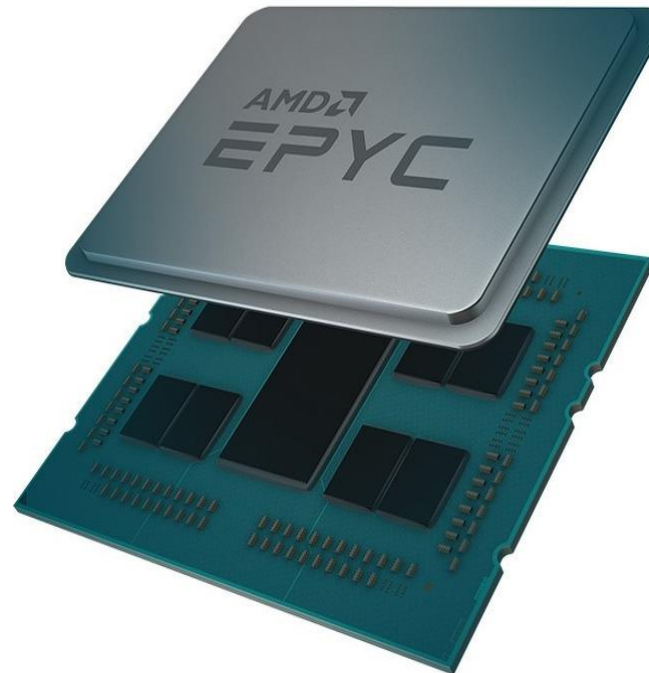
4 flip-chip placement steps

9 flip-chip placement steps

> 30 die placement steps
including hybrid and flip-chip



Source: AMD



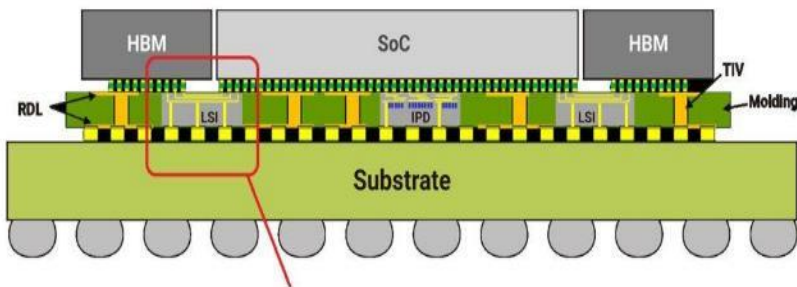
New Process Technology: Embedded Bridge Die Attach Stitching Together Processor Chips with Wafer Level Fan-out Bridges

First embedded fan-out bridge devices/assembly systems introduced in Q1 2022

Multiple customers developing (AMD, TSMC, Intel, Amkor, ASE, SPIL, Deca)

Molded Fan-out Interposers

- Connects chiplets using slices of Si (bridges) embedded in a molded fan-out wafer
- Lower cost and more flexible compared to Si Interposers
- Requires sub-micron chip-to-wafer attach of embedded die

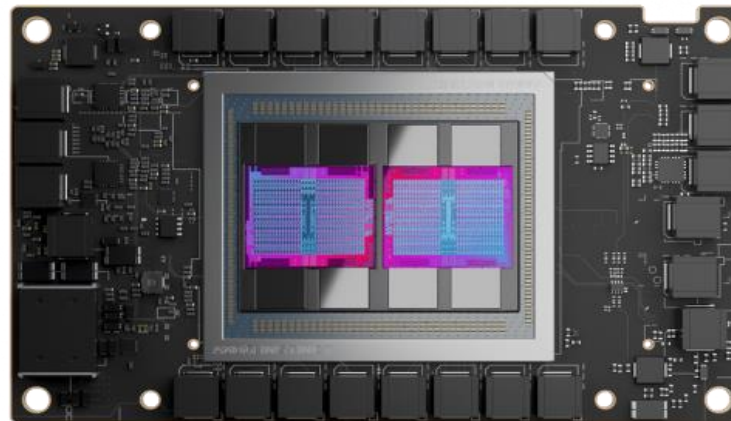


CoWoS-L, with embedded Local Silicon Interconnect bridge
"BEOL, chip-last assembly"

Source: TSMC

AMD Instinct MI200 GPU

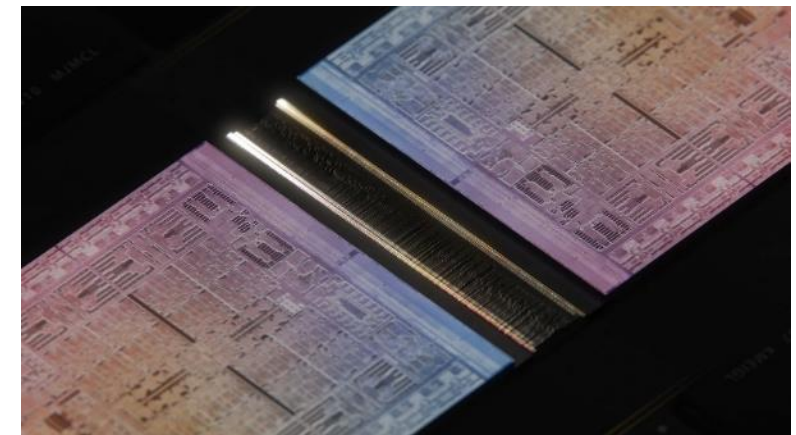
- World's first multi-chip GPU
- Based on TSMC 6nm process
- First main-stream application of wafer level fan-out interposer with embedded Si bridge



Source: AMD

M1 Ultra chip

- High end desktop CPU
- Embedded Si bridge to connect 2 M1 Max chips in single package
- High speed digital bus, 25um pitch, connects adjacent die with 2.5TB/second of bandwidth



Source: Apple

Si Photonics market forecast to grow by 28% CAGR (2021 – 2027)*

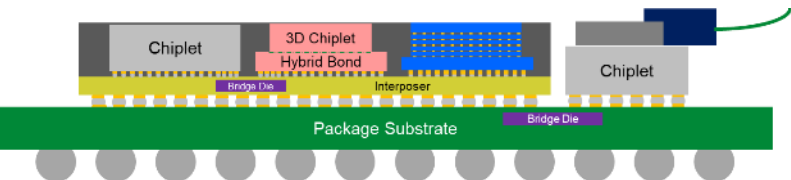
Optical Transceivers

- Assembly of lasers, photodiodes, sub-assemblies
- Besi has strong market share



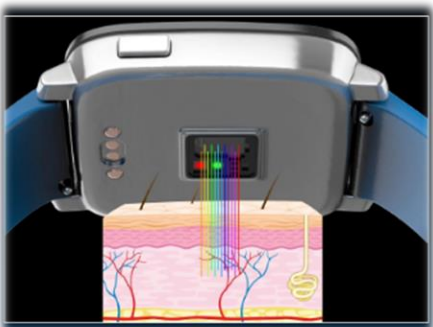
Co-Packaged Optics

- Optical chiplets brings fiber to the package substrate
- **Requires higher accuracy, chip-to-wafer assembly**

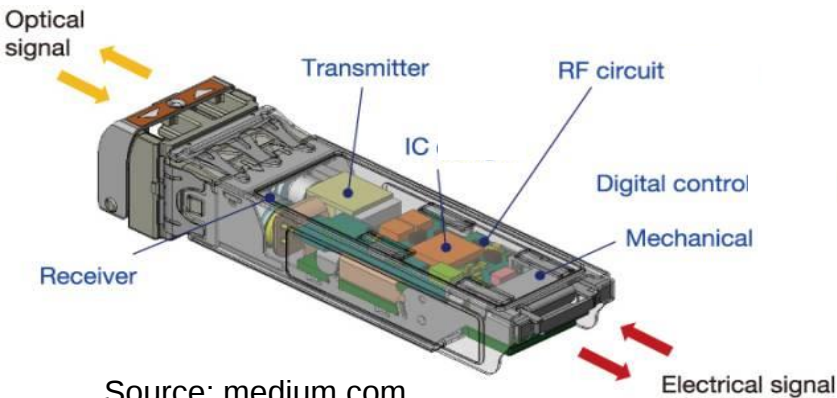


Wearables and Sensors

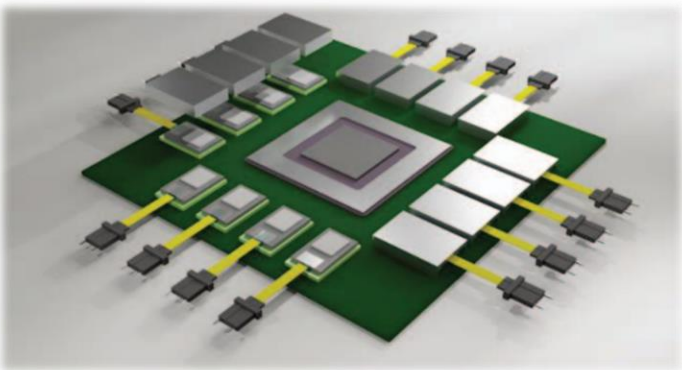
- New photonic based bio sensors



Source: Rockley Photonics



Source: medium.com



Source: ASE, ECTC 2022

- LIDAR for mobile phones and wearables



* Source [Silicon Photonics Market Size, Share \(2022 - 27\) | Industry Forecast \(mordorintelligence.com\)](#)

Mobile: Increasing 5G Adoption is Primary Growth Driver Will Generate New Smartphone Applications and Features

5G rollout is progressing, still mid-cycle adoption rates

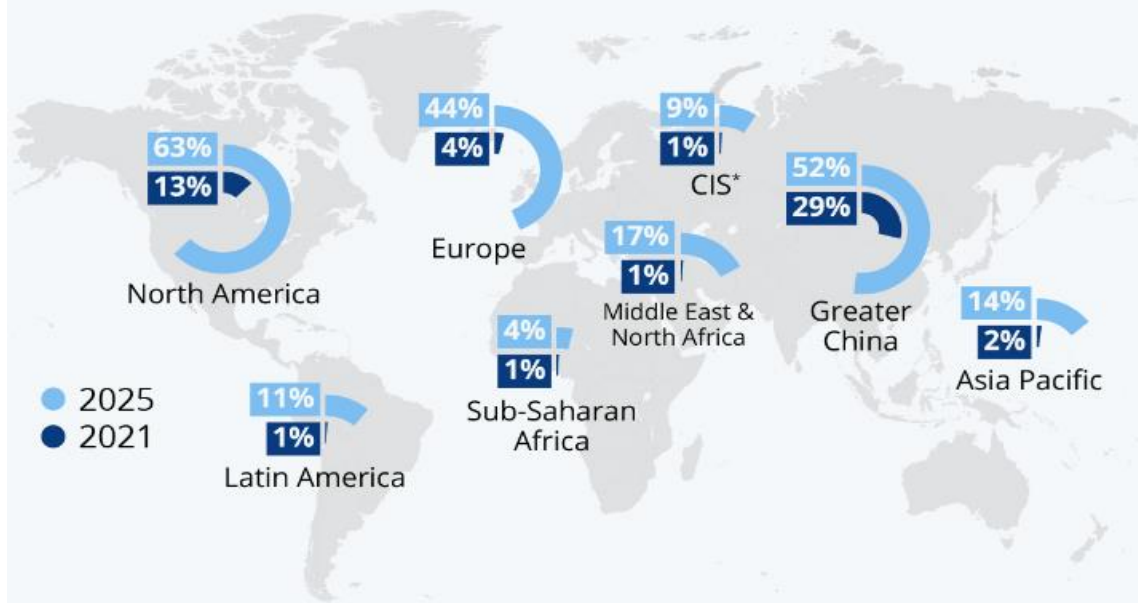
- mmWave 5G deployment and 6G research in progress

Mobile data traffic is growing rapidly

- Growth in new features and functionality requires new advanced assembly systems

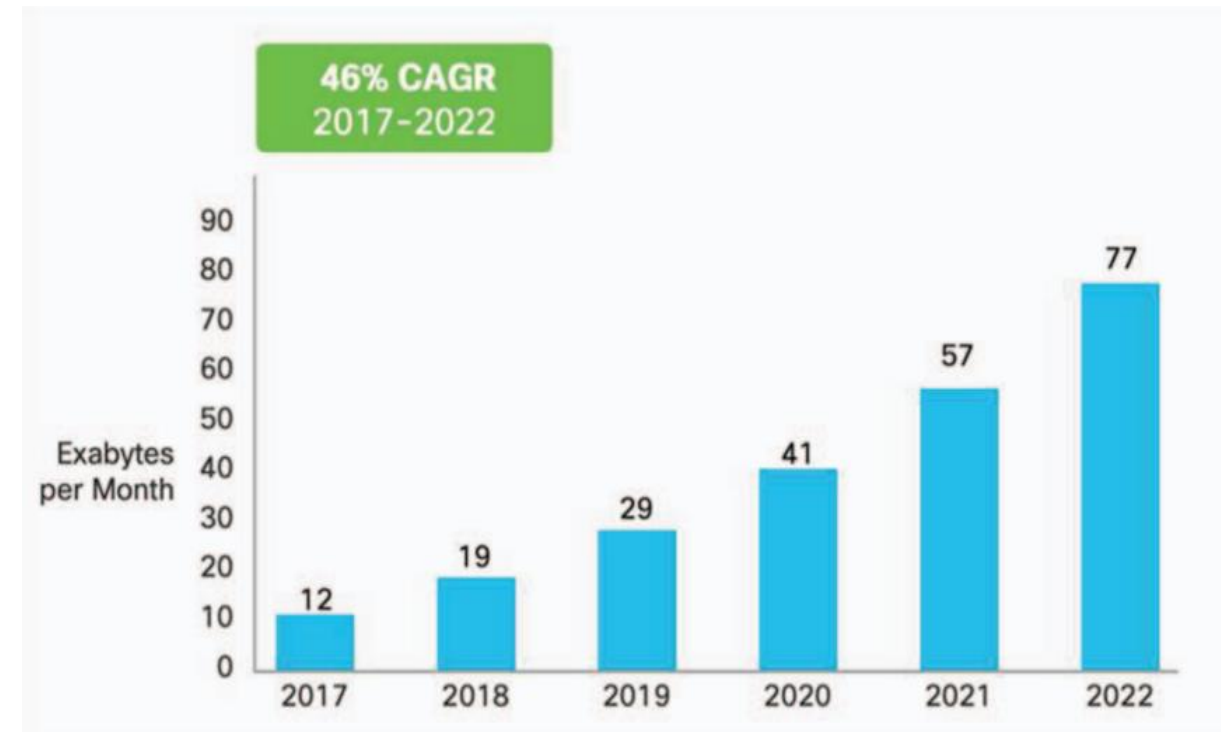
The State of 5G

Estimated worldwide 5G adoption as a share of total mobile connections (excl. IoT)



Source: IDC

Global mobile traffic growth 2017-2022



Source: Cisco, 2022 ECTC

mmWave 5G → 6G

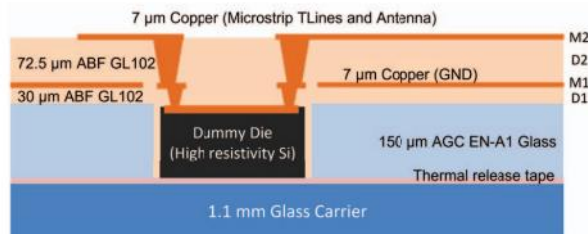
- Deployment of mmWave small cells and smart repeaters
- **Next generation RF SiPs with new materials, features & direct Cu interconnects**



Source: Qualcomm



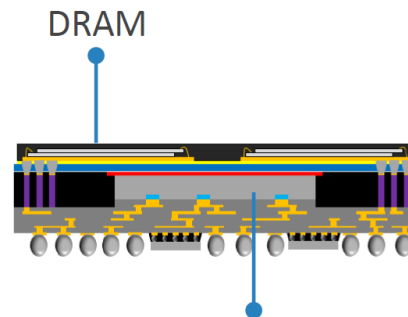
Source: Prismark



Source: Georgia Tech, 2022 ECTC

3DIC for Application Processor

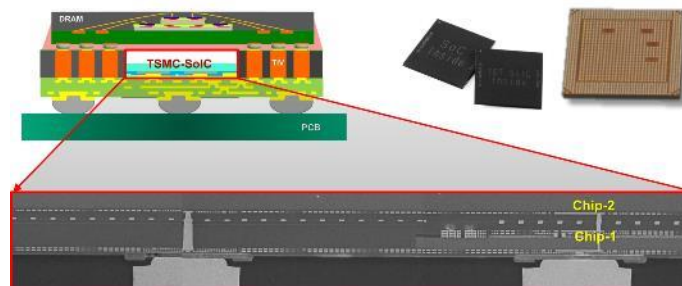
- More functions like AI to be integrated in the AP chip
- Facing Moore's Law scaling limits



Source: Yole

SoC die

- 3DIC with **hybrid bonding** may enable next gen APs



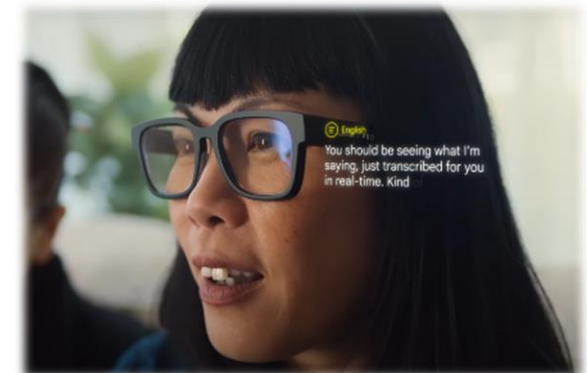
Source: TSMC

AR Glasses

- In development by all top consumer electronics players
- Requires extreme miniaturization, 3DIC, TCB, advanced molding



Source: Qualcomm

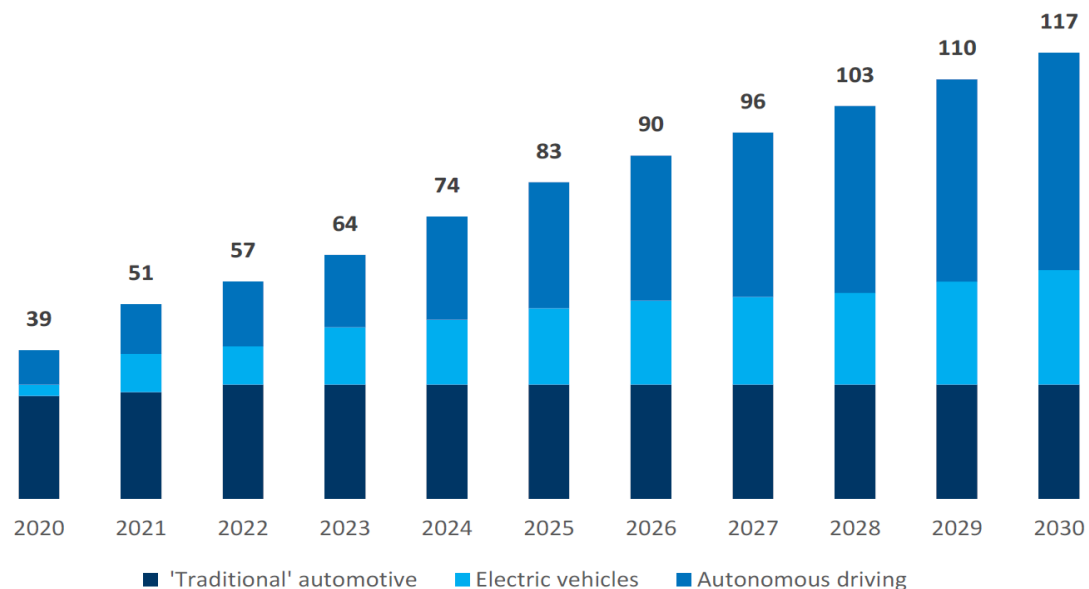


Source: Google

Automotive: Growth of EV and Autonomous Driving Will Increase Semiconductor Content and Cost per Car

Majority of cars produced by 2030 will have an EV drive train

IDC Automotive Semi Market Forecast (\$ bn)



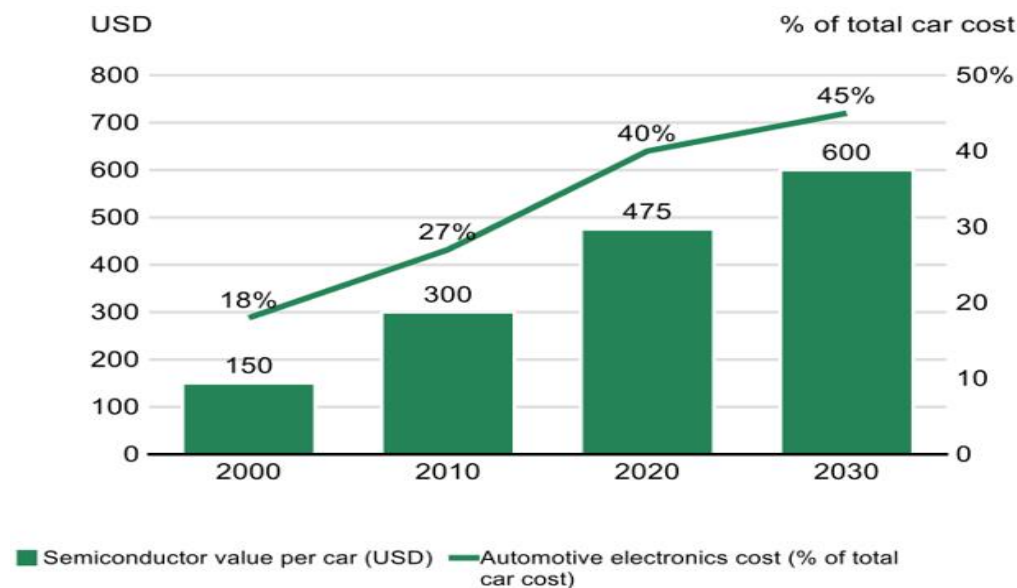
Source: Gartner, ASML Position Paper – European Chips Act

12% CAGR in automotive semi sales 2020 – 2030

- Semis for electrification to grow by 26% CAGR
- ADAS Semiconductors to grow by 20% CAGR

Almost all will have some level of autonomous driving

Semiconductor content per car is increasing



Source: IHS Markit and Deloitte Insights, July 2020

Upward trend anticipated to continue

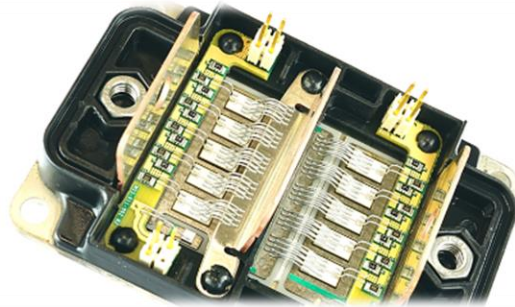
- More sensors: cameras, radar, ultrasonic, LIDAR
- Increased use of AI, V2E connectivity

Advances in Power Device Packaging for Vehicle Electrification

SiC replacing IGBTs in high power conversion
Increased power efficiency results in longer EV range

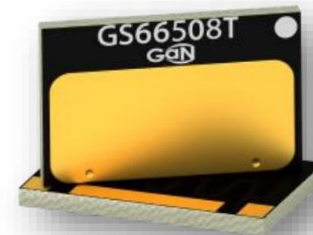


Source: Cree

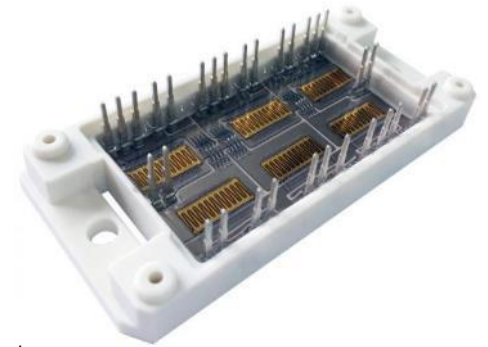


Source: Wolfspeed

GaN MOSFETs highest frequency power switching
50% smaller onboard chargers and DC/DC converters



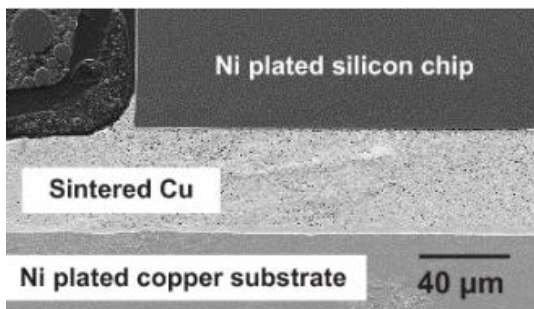
Source: GaN Systems



Requiring new die attach and packaging methods

Die attach

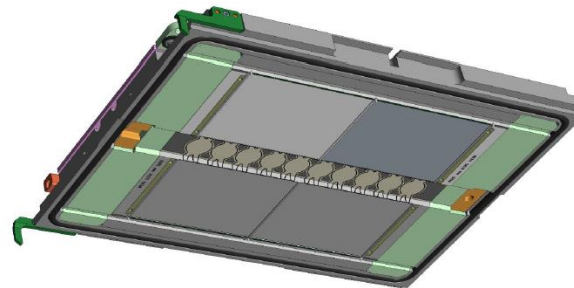
Sinter bonding



Source: 2018 ESTC

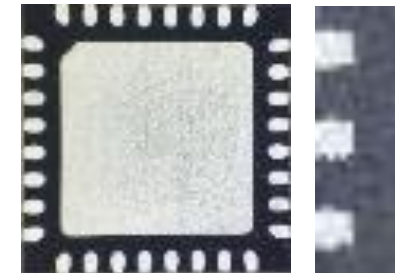
Packaging

Advanced molding



Plating

Wettable Flank QFN



Autonomous Driving Will Drive Growth in Both Advanced and Legacy Packages

Higher levels of driving automation

60% of new cars to have partial automation by 2030



Source: Voestalpine

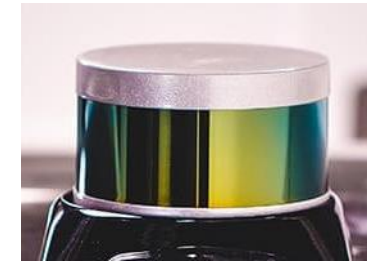
Using more cameras and sensors

Camera



Source: ST

Lidar



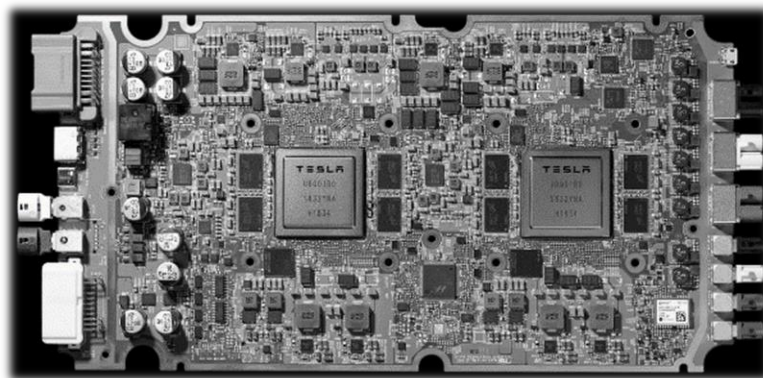
Source: mzwmotor.com

Radar Tx/Rx



Source: NXP

Requiring more edge computing power in the car

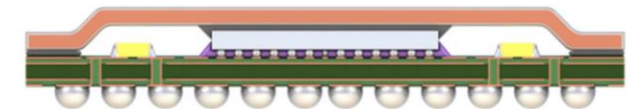


Source: Tesla

Driving growth in both advanced and legacy packages



Source: Infineon



Source: Amkor

Besi Well Positioned to Capture Next Generation Opportunities



Multiple long term drivers for secular growth

- Computing: Big data, AI, edge computing, photonics
- Mobile: Continued roll-out of 5G, wearables, and deployment of mmWave 5G
- Automotive: EV and autonomous driving

Slowing of Moore's Law drives innovation in chiplet architectures

- Chiplets = more die placement steps = higher capital intensity
- Besi is well positioned with leadership in hybrid bonding and sub-micron die attach

New mobile technologies on the horizon

- New wearable devices like AR glasses with challenging form factors & advanced cameras
- Potential adoption of hybrid bonding in mobile processors
- 3D IC integration, advanced camera systems and 3D sensing

Transition to EVs with autonomous driving

- New SiC and GaN power devices requiring new die attach processes
- Increase in sensing and on-board computing content for safety and automation
- Requires advanced process control



IV. MAINSTREAM DIE ATTACH

Christoph Scheiring
Senior VP Die Attach



Industry Leading Die Attach Equipment Portfolio

Multi-Module Attach



- 2200 evo
- 2200 evo *plus*
- 2200 evo *hS*
- 2200 evo *advanced*
- 2200 evo *hf* **Q1'22**

Epoxy Die Attach



- 2100 hS
- 2100 hS *i*
- 2100 sD *advanced i*
- 2100 hS *ix* **Q4'21**

Flip-Chip



- 8800 FC Quantum *adv / sigma*
- 8800 FC Quantum *hS*
- 8800 CHAMEO *advanced / PLP*
- 8800 FC CHAMEO *Ultra* **Q2'22**
- 2100 FC *hS*

Soft Solder Die Attach



- 2009 SSI
- 2100 SSI **Q2'22**

Continuously Upgraded for New Applications

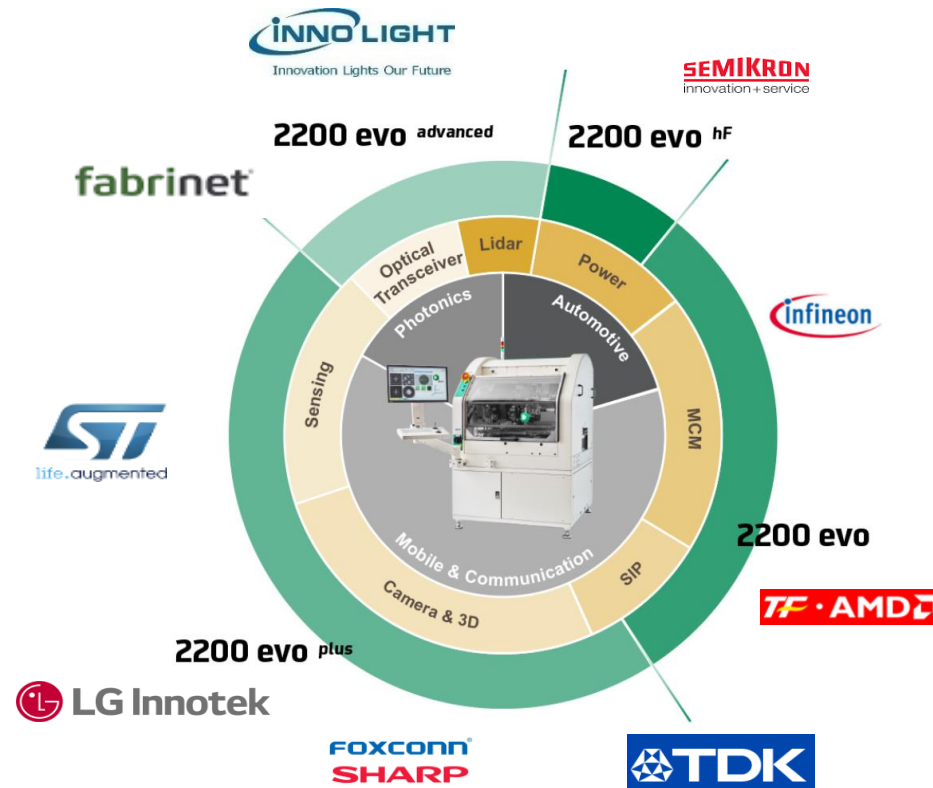
> 6,500 Units Shipped



Key competitive advantages

- Multi-die, multi-wafer
- High Accuracy and high speed
 - 1.5 μm in development
- Highly configurable
- Broad range of applications
- Rapid R&D to production

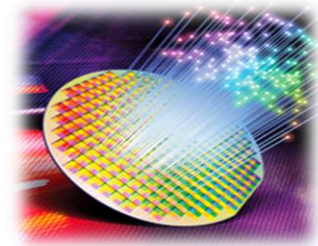
Target Markets & Customers



New Developments 2022

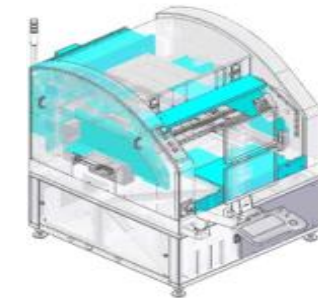
Increase accuracy

For SiPH market
(transceivers)



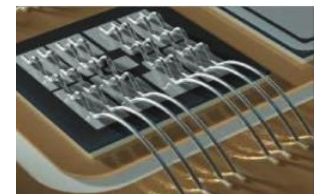
Increase Cleanliness

Achieve front-end
levels for advanced
camera modules



Increase Bondforce

For large die
power devices



Source: Semikron

2100 Epoxy Die Attach: Industry Leading Platform

Highest Speed and Accuracy for Single Die Placement

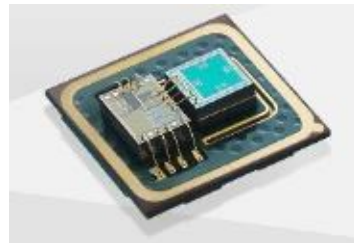
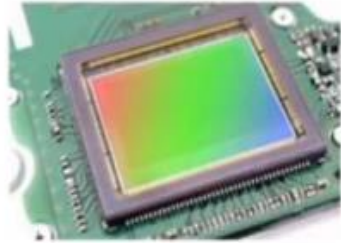


> 4,000 Units Shipped



Target Markets & Customers

- **Mobile, 5G:** PA, RF front end modules, Sensors, PMIC, analog
- **Automotive:** MEMS and Sensors, Auto CIS
- **Storage:** NAND
- **Industrial:** Analog, power, MCU



Key competitive advantages

- Industry leading accuracy and speed
- Precise bond line thickness control
- Confocal scanning for real time material height and epoxy volume compensation
- Ultra-thin die and cleanliness
- Automation: AGV loading

New Developments 2022

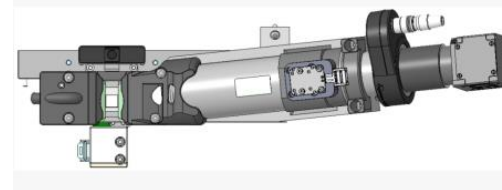
Focus: Automotive power, advanced quality control and 5G performance

3D Dispensing & Epoxy Volume Control



Auto CIS

6 Side Die Inspection



Automotive quality

Automation & Advanced Diagnostics



Control HW & Vision & Dispenser, one button setup, AI assisted vision

Industry Leading Flip-Chip Product Portfolio

Advanced Flip-Chip and Fan-out 8800 CHAMEO



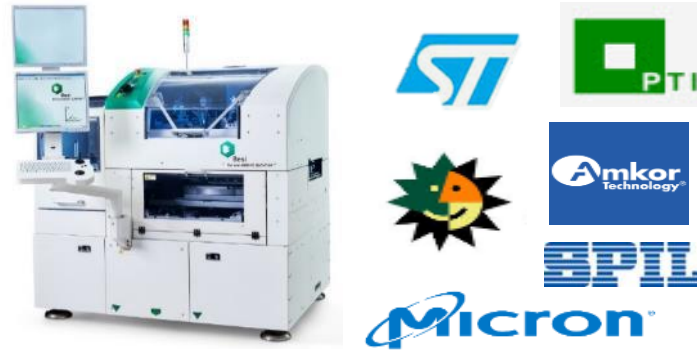
fcBGA, 2.5D, FOWLP

- Accuracy: < 3 (1) μm
- Throughput: 10,000 UPH
- Die size: 40mm, 300mm substrate
- EFEM Loader, Factory Automation
- ISO 5 cleanliness

New Developments 2022

- Advanced bondhead with V-axis
- Granite base
- T&R and wafer

High Speed Flip-chip 8800 QUANTUM



fcCSP, 5G SiP, Memory

- Accuracy: < 4 μm
- Throughput: 14,000 UPH
- Die size: 14 mm in high speed mode

New Developments 2022

- Quattro BH and Eject system

2100 FC hS

Lowest cost of ownership



FCoLf / QFN / Led / SiP

- Accuracy: < 8 μm
- Throughput: 15,000 UPH
- Die size: 0.3 -20mm

New Developments 2022

- Latest i-HW & features (vision, accuracy, GUI)

2100 Soft Solder System: Quantum Step Forward for Automotive and Industrial Applications

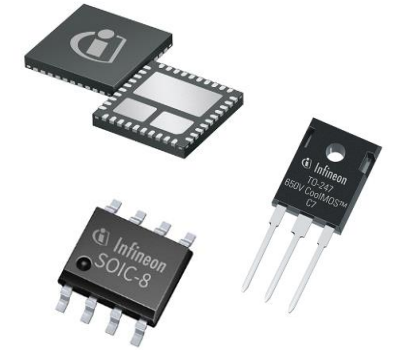


Next Generation Soft Solder



Target Markets & Customers

- **Automotive:** High Rel Power packages, SiC
- **Industrial:** All power devices, IGBT, IPM, Clip Bonding



Source: Infineon Technologies

Key competitive advantages

- Leading soft solder process
 - Low oxygen level
 - Lowest gas consumption
 - Fully automotive qualified
- XLF leadframe handling
- POR for key automotive IDM

New Developments 2022

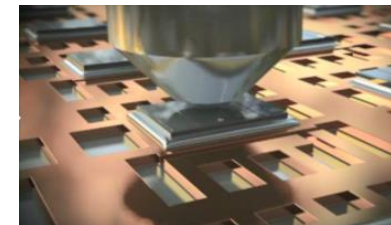
Common platform with 2100 epoxy system to extend capabilities and reduce cost

Qualification



Wide leadframe
Lowest gas consumption

Process Superiority



High bondforce for diffusion soldering
Combined dispense & PPM

Sustainability



Reduce energy and
materials consumption

Die Attach Growth Opportunities

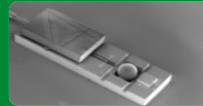
Multi-Module Attach



Mobile
Sensing



Optical
Tranceivers



High Power
Modules



Epoxy Die Attach



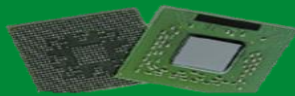
MEMS / RF



Advanced FC & Fan Out



FC Memory



FOWLP / HPC



Soft Solder Die Attach



Auto/Industrial
Power



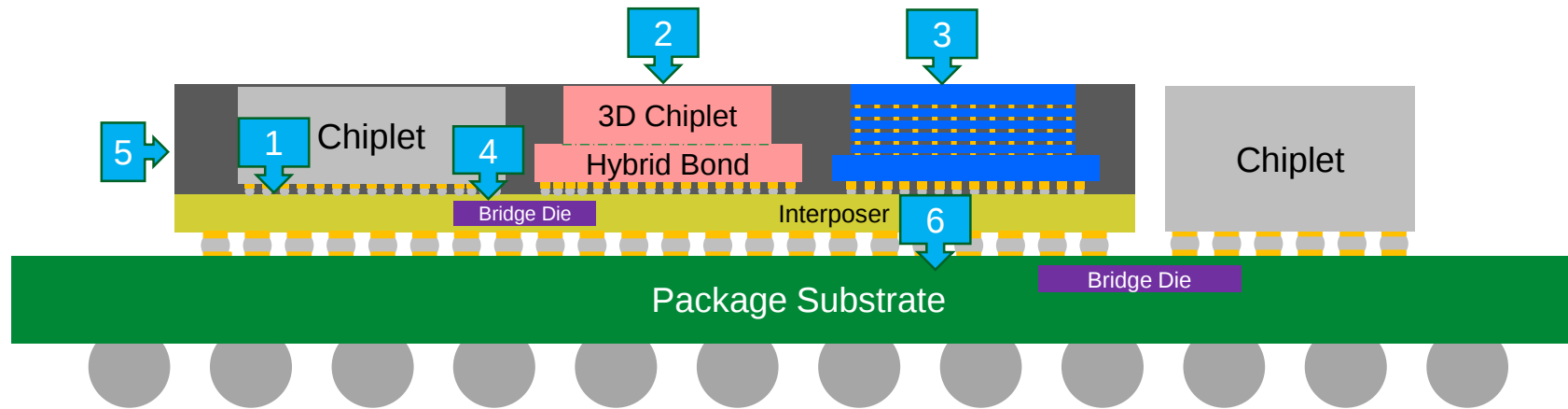


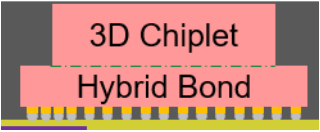
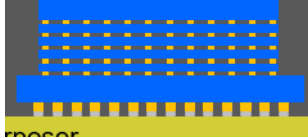
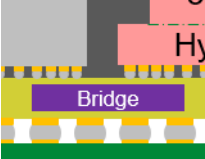
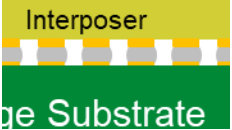
V. WAFER LEVEL ASSEMBLY

Peter Wiedner
Senior VP Sub-Micron Die Attach

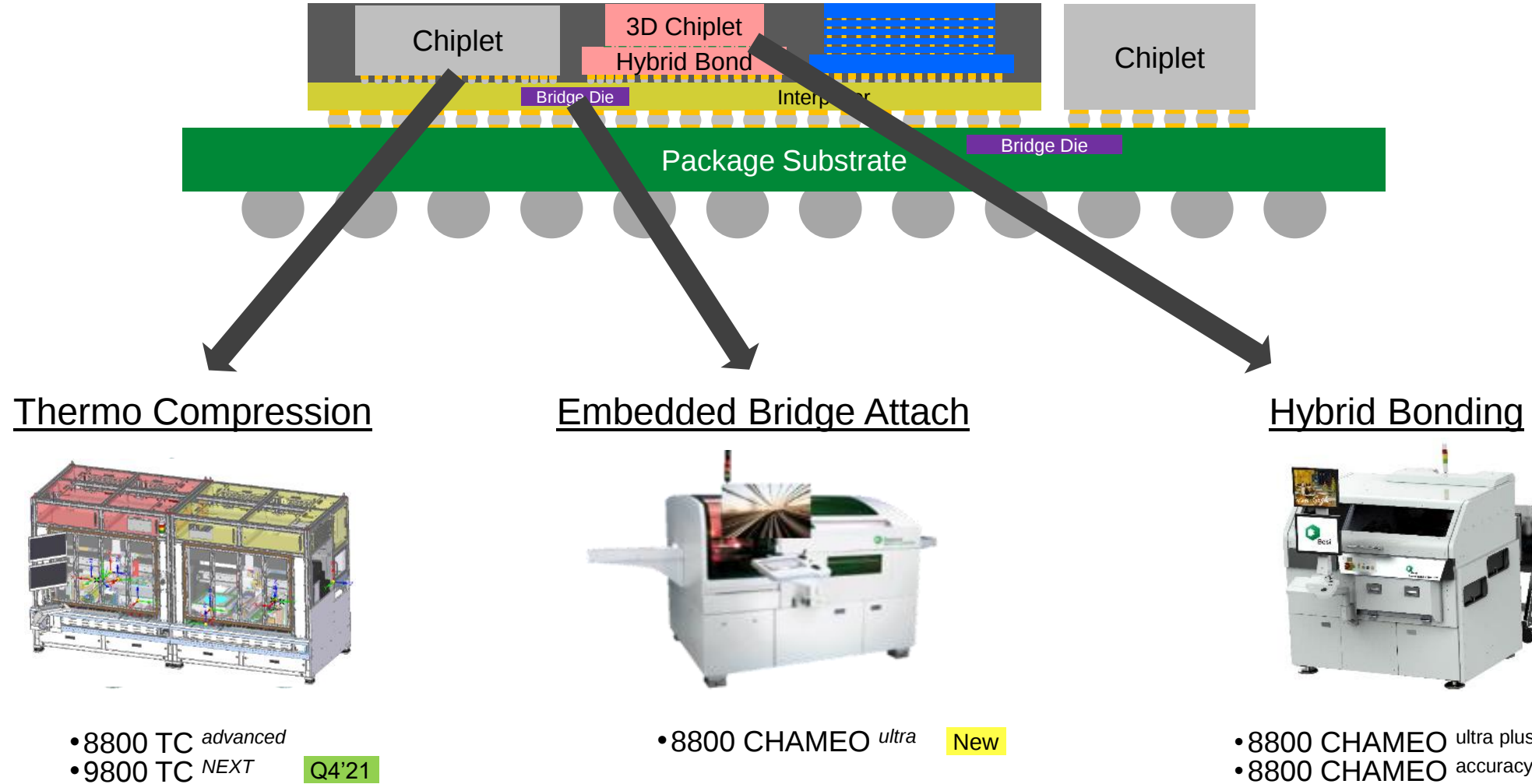


Portfolio of Sub Micron Accuracy Die Bonding Systems for Wafer Level Logic and Memory Applications



1	2	3	4	5	6
Chip to Wafer TCB	Hybrid Bonding	High Bandwidth Memory Stacking	Embedded Bridge Die Attach	Wafer Level Die Molding	HD Interposer to Substrate
					
TC Next C2W	8800 Chameo Ultra Plus	8800 TC Advanced 8800 Chameo Ultra+	8800 Chameo Ultra	FML	2200 evo

Three Principal Die Bonding Platforms



Next Generation TCB System Targeting C2W Applications for HPC To Be Introduced in Q4-22



9800 TC^{Next}



Besic
9800 TC ^{next}

Target Markets & Customers

- **Computing:** HPC, Heterogeneous Integration
Si interposer attach
- **Memory:** HBM stacking



SAMSUNG

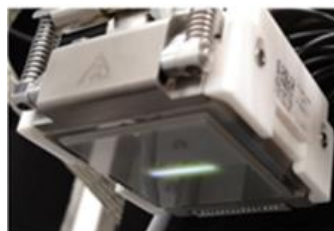


Key competitive advantages

- Both chip-to-substrate and chip-to-wafer capabilities
- Flexible material handling
- Bond collapse detection
- **Submicron accuracy**
- **Up to 70mmx70mm die size**
- **Ultra-low gas usage**

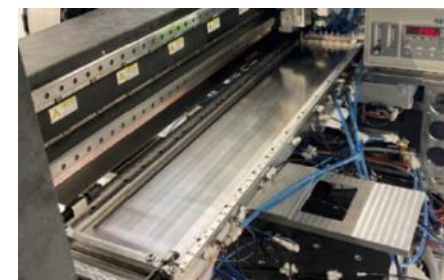
Key Features/Functions

9800 TC^{Next}



Sub-micron accuracy
for chiplets

Next Gen Process Chamber



Ultra low gas consumption

Fluxless process



Smaller pitches
requiring fluxless process

Recently Introduced Embedded Bridge Die Attach System Critical to Power Chiplet and Other Wafer Level Architectures

First Bridge Die Attach System Shipped in Q2-22



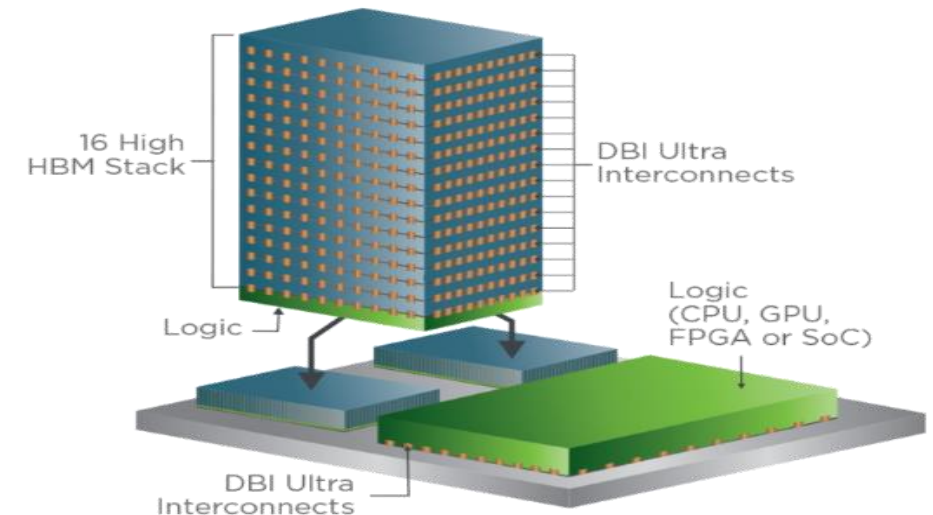
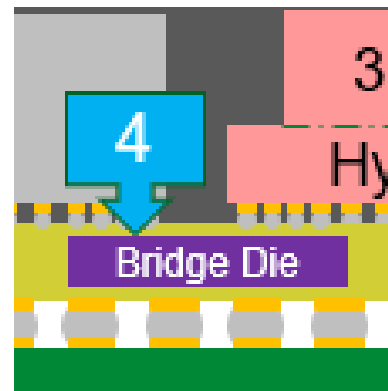
Target Markets & Customers

- **Computing:** HPC, Heterogeneous Integration
Si interposer attach



Key competitive advantages

- Based on market leading BESi FC platform
- **1 μ @ 3 sigma local accuracy**
- **Face up / Face down**
- **C2S / C2W incl. EFEM loading**
- Full factory automation
- ISO 5 clean class
- Full Auto tool changer



Heterogeneous integration requires wafer level fan out technology to make connections

8800 Chameo Ultra Plus: Reflects Industry Shift To Smaller, Integrated, Heterogeneous Chip Designs



Leading Hybrid Die Bonding System on Market



- Direct Cu-Cu Interconnect
- Design Flexibility
- Lower Cost of Ownership
- Ultra-High Bandwidth & Speed

Target Markets & Customers

- **Computing:** Chiplet integration for HPC
Heterogeneous integration
- **Memory:** High density 3D NAND
- **Mobile:** AP & RF SiP modules



NVIDIA



AMD

SAMSUNG



Qualcomm

Key competitive advantages

- Patented Van Gogh bond head and vision system
- **< 200 nanometer accuracy**
- **High speed: ~2000 UPH**
- High production yield achieved
- Front-end clean room standard
- Full front-end automation including tool changes

New Developments 2022

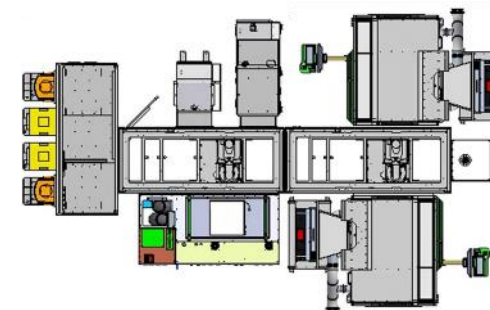
Q1

Volume Production Started



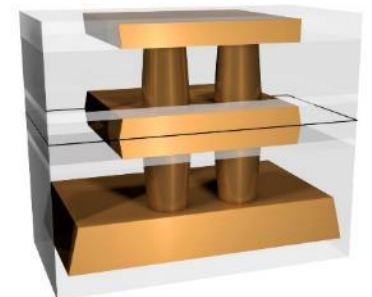
Q3/4

Cluster Line Integration



Q4

100 nm accuracy



Applications Driving Hybrid Bonding Growth

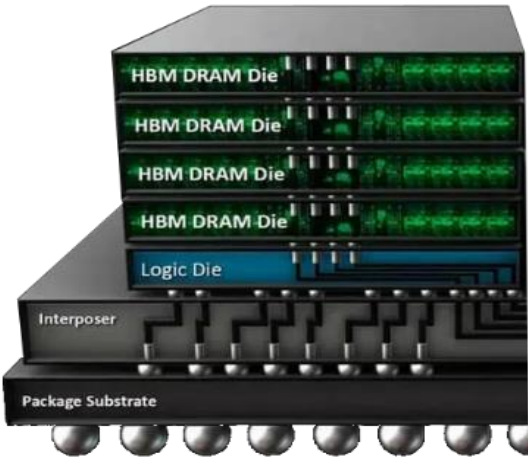
Logic



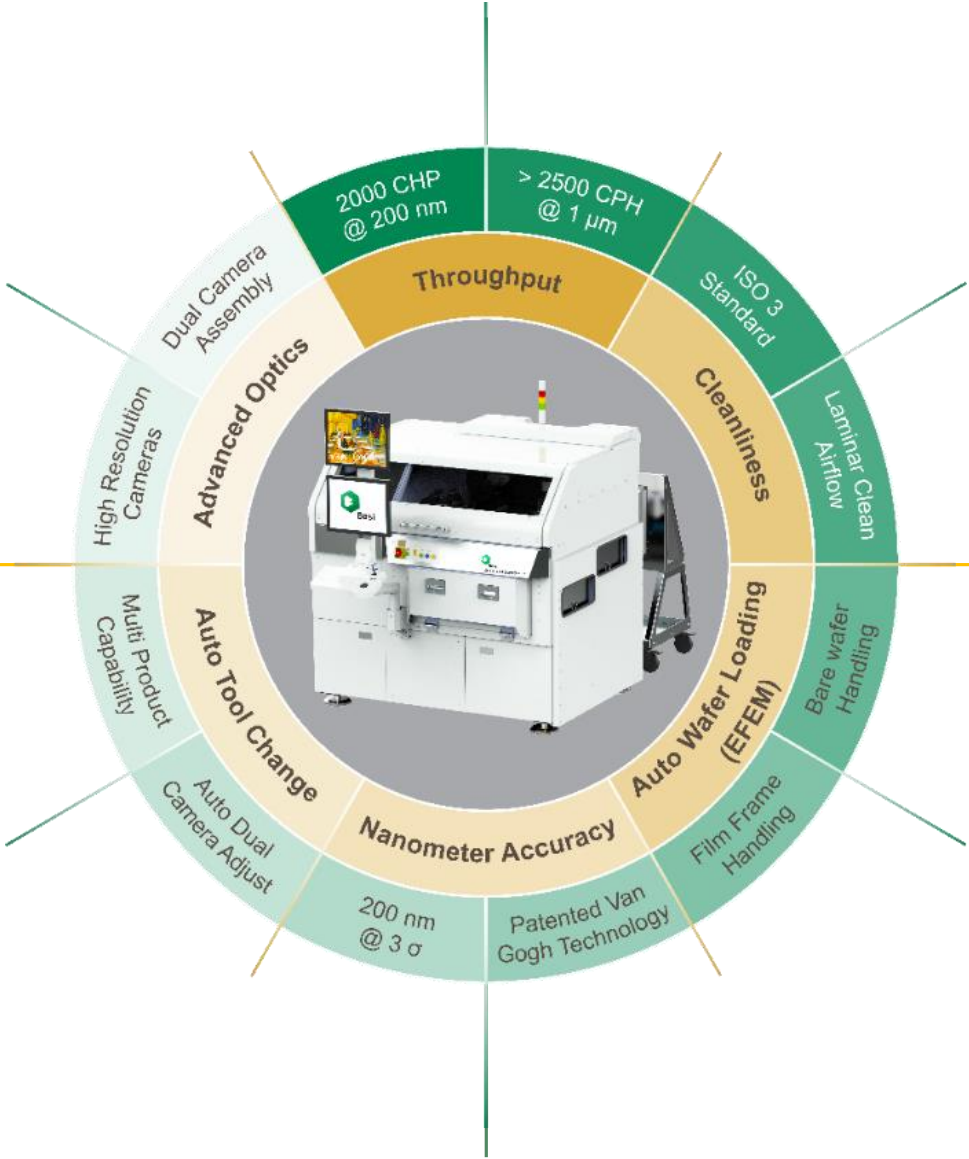
Sensors & Display



Memory



Mobile

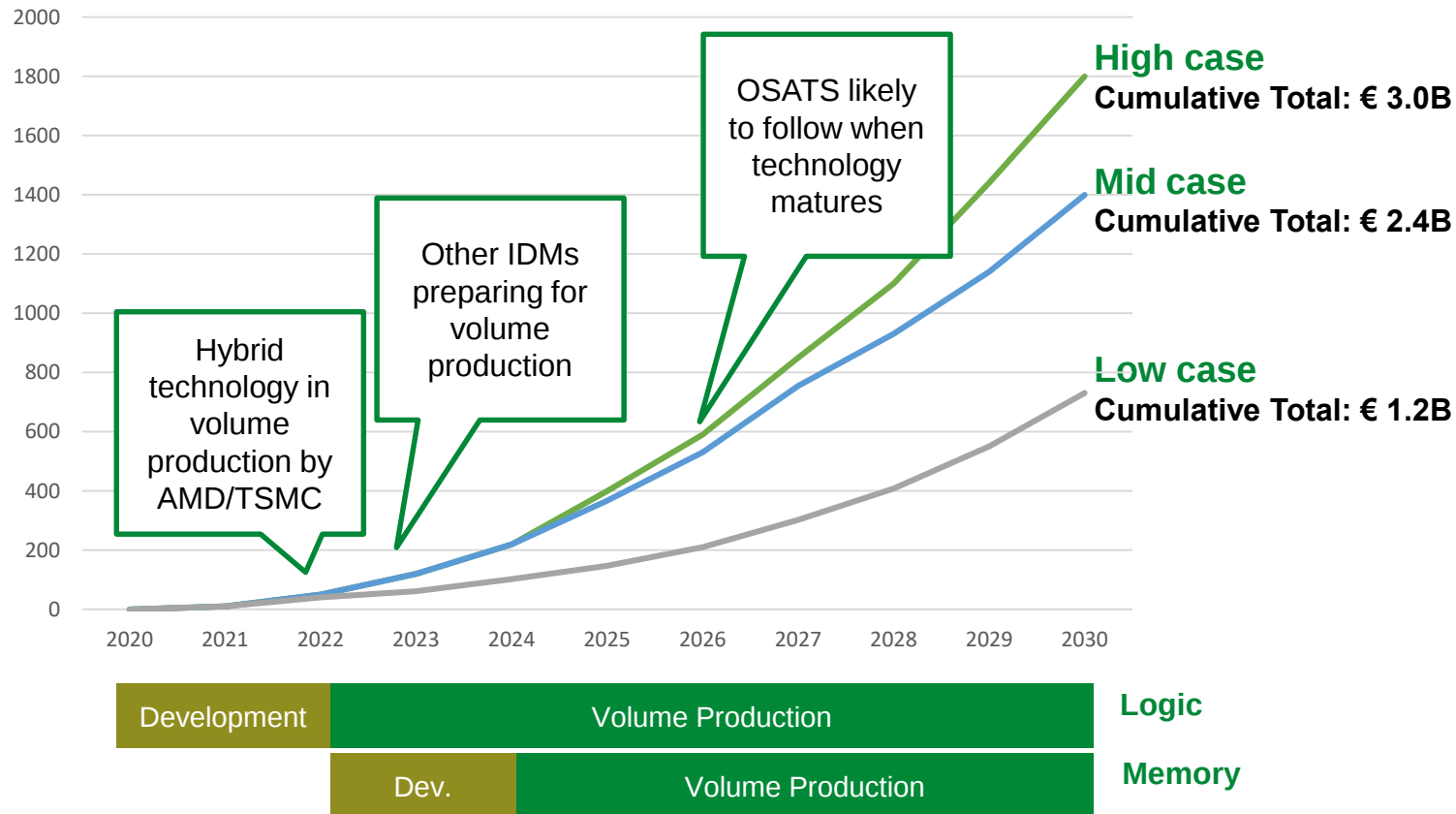


Hybrid Bonding Adoption Gaining Traction

Hybrid Bonding Equipment Market

Estimated 700 – 1,800 systems by 2030

Total # of installed back-end machines for hybrid bonding



Source: Besi estimates

- Hybrid now on radar of all major semi producers
- Not question of if, but when and how large the market opportunity
- Upside market potential expanded
 - Tracking to mid case currently
- **Expected rollout sequence:**
 1. Logic
 2. Memory
 3. Mobile
 4. Subcontractors

Logic customers have moved to volume production:

- BESi moved from proof of concept to quantity shipments
- AMD's first hybrid bonded 3D chiplet-based processor (RYZEN) commercially available
- Multiple customer engagements

Memory is starting proof of concept:

- First hybrid system shipped to major memory IDM in Q2-22

Research Centers:

- Expanded activities and customer engagement at Singapore Center of Excellence
- BESi and IMEC signed JDA

Inside BESi:

- Expanding capacity to potential 15-20 systems per month
- Production leadtimes reduced from 6 months to 3 months
- Development & service staff organized to support customer production in US & Taiwan
- Preparing cluster tool solution with AMAT to enable next level productivity



VI. PACKAGING/PLATING

Jeroen Kleijburg
Senior VP Packaging



Best in Class Packaging and Plating Equipment Portfolio. Focused on Leading Edge Applications and Customers



5G and Wearables



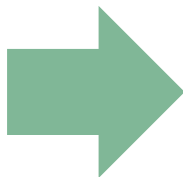
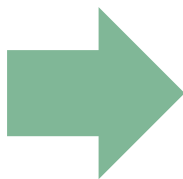
IoT/Computing



Automotive



Storage and Network



Substrate Molding



AMS-LM

- Two sided substrate molding
- Exposed die;
- Wearables (SIP)

Substrate Singulation



FSL

- Substrate strip singulation
- Sorting
- Stepcut **New**

Wafer & Panel Molding



FML

- Wafer molding
- Panel molding

Leadframe Molding



AMS-X

- HD Leadframe **New**
- Power Devices

Trim and Form



FCL-X/P

- Leadframe trim & form
- Sorting

Plating



- Leadframe
- Solar
- Film & Foil
- Battery
- Chemical Deflash
- Wettable Flank

Q3'21
New

Molding: AMS LM Substrate Molding: Leading Exposed Die System for 5G and Complex 3D Molding Applications

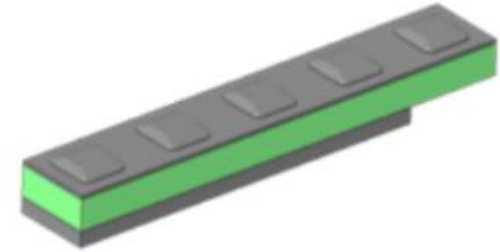


350+ Systems Shipped



Target Markets & Customers

- **5G** : Advanced RF front-end modules
- **Wearables** : SiPs with intricate 3D designs
- **Memory** : Stacked Die and FC DRAM 5



Key competitive advantages

- Best in class COO
- Lowest power usage and weight
- Standard for thin die molding
- Exposed die molding (90% share)
- Dynamic clamp force control
- Board thickness compensation
- Double sided molding (5G FEM)

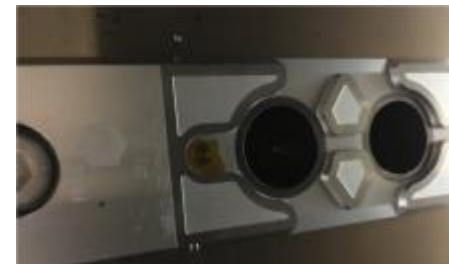
New Developments 2022

Low Electrostatic discharge <50V/Inch



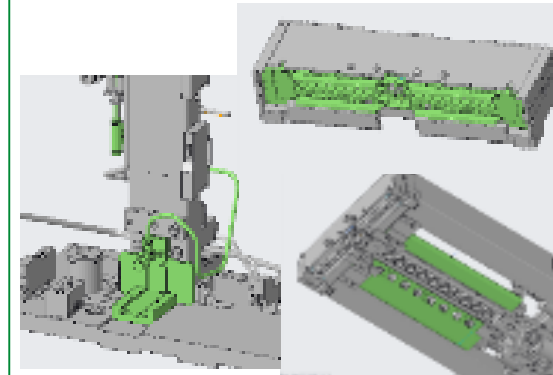
Safe for MEMS and RF

Low transfer pressure



Safe for MEMS and XTALS

Particle reduction



FML Wafer Level Molding For Exposed Die Applications Including Hybrid Bonding

Introduced in 2018

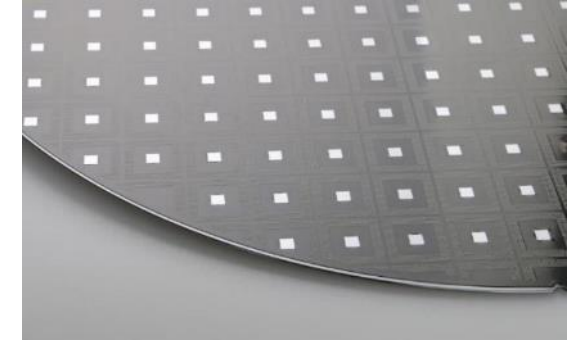


Target Markets

- **Computing:** Chiplet integration for HPC
Heterogeneous integration
- **Mobile:** 3D Wafer level fan-out



Wafer level mold with exposed die



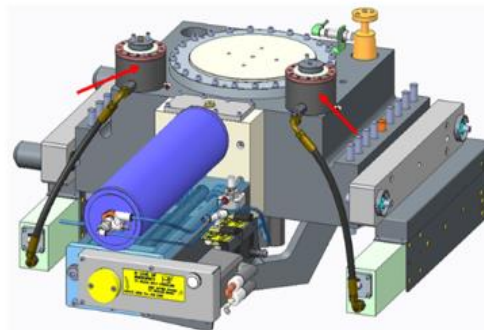
Key competitive advantages

- Exposed die wafer molding
- No die swim
- Narrow gap filling < 50 μm
- Dynamic clamp force control
- Mold planarity below 5 μm
- High precision wafer placement
- 150 ton capability

New Developments 2022

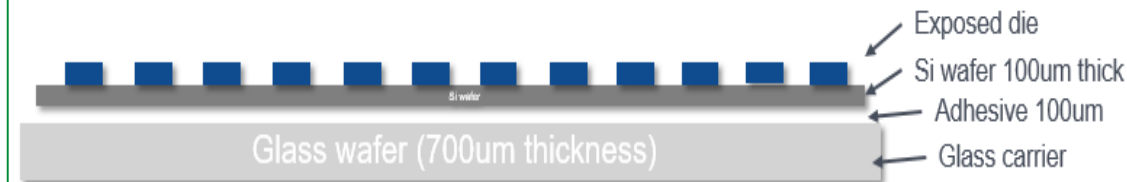
Auto leveling

Precise thickness across wafer



TSV Wafer molding

Exposed die molding to encapsulate hybrid bonded die



Singulation: FSL Stepcut Leadframe: Power and SIP Packages for Automotive and Server End Users. Gaining Market Traction

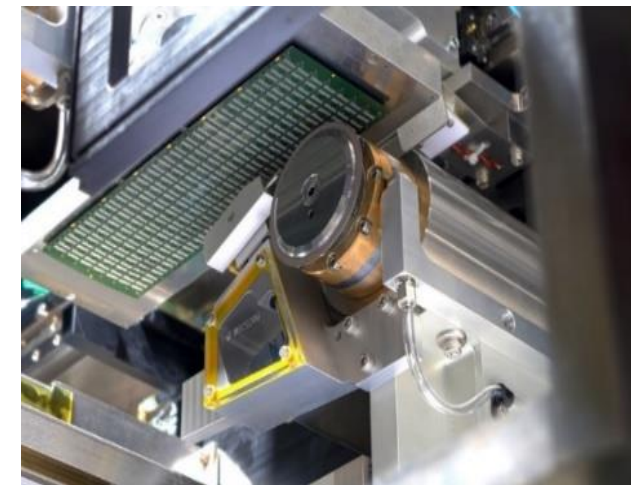


Singulation



Target Markets

- **Server** : System in packages
- **Automotive** : SOIC and TSOP packages
- **Memory** : Stacked Die and FC DRAM 5
- **5G** : Advanced RF front-end modules



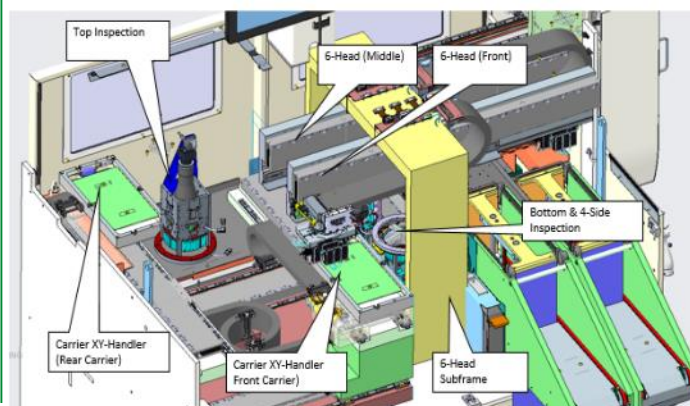
Key competitive advantages

- Step-Cut: $\pm 20\mu\text{m}$ with $\text{Cpk} > 1.33$
- Size & Offset: $\pm 25\mu\text{m}$ with $\text{Cpk} > 1.67$
- Warpage Handling (short): $< 12\text{mm}$
- Warpage Handling (long) $< 18\text{mm}$
- Conversion time less than 5 minutes
- Stack magazine offloading with step cut
- 35% less water consumption

New Developments 2022

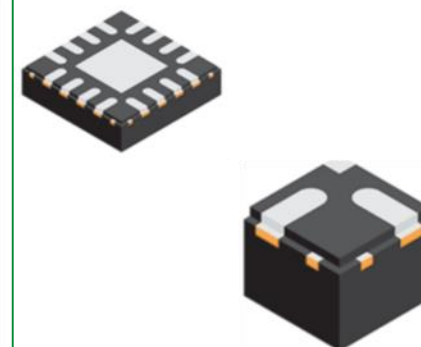
High speed sorting

> 45K UPH with tray offload



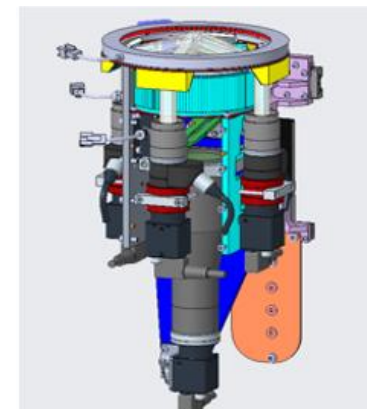
Step cut

Increases reliability



6-sided inspection

Increases reliability



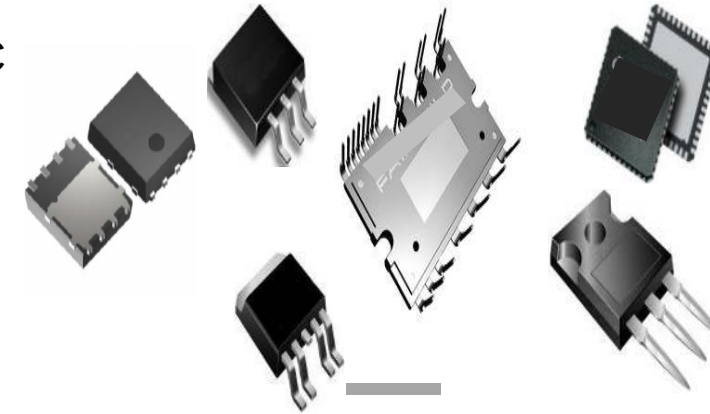
Molding: AMS-X Leadframe Molding: Power and SIP Packages for Automotive and Industrial Market

Introduced in 2021
First systems in production



Target Markets

- **Automotive:** High Rel Power packages, SiC
- **Industrial:** All power devices, IGBT, IPM

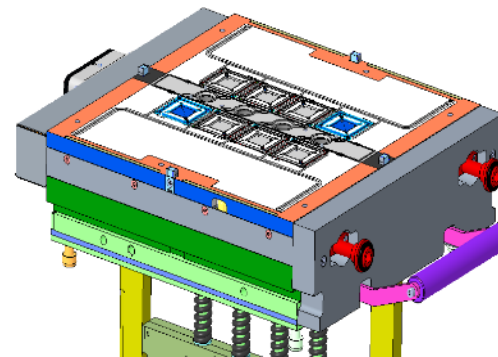


Key competitive advantages

- 20% less energy consumption
- 12% less compound loss
- Modular concept (modules used from T&F and singulation)
- High cavity vacuum of 50 mbar
- 4 individual clampforces
- No vibration due to low weight
- Leadframe size up 125 mm

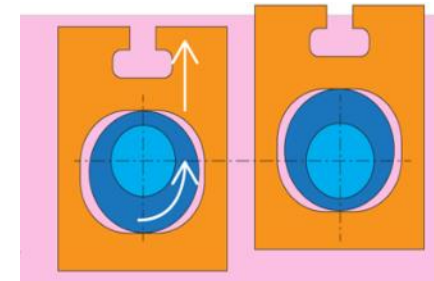
Improved vacuum control

< 50 mbar in sleeve

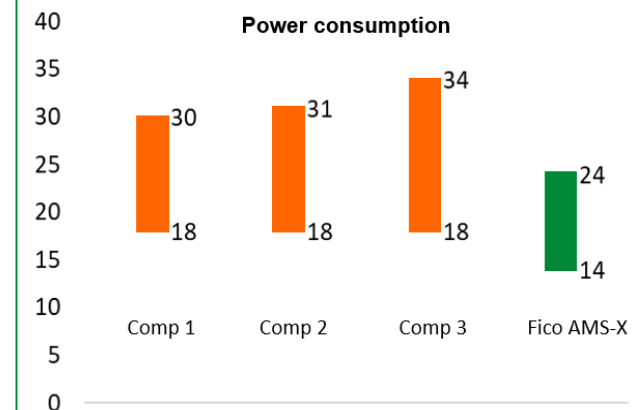


Independent ejector bed

Prevents delamination



Reduced power consumption



Trim & Form: Fcl-x for Power and SIP Packages for Automotive and Server Markets

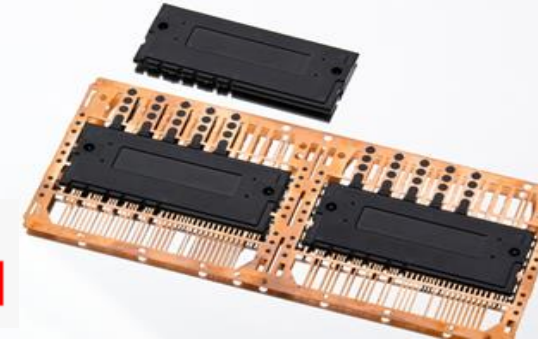
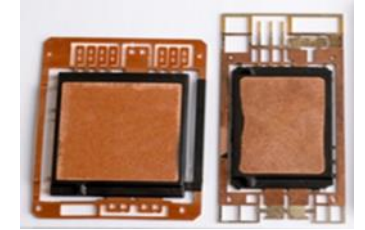


1500+ Systems Shipped



Target Markets

- **Server** : System in packages
- **Automotive** : IGBT, SO and TSOP packages



Key competitive advantages

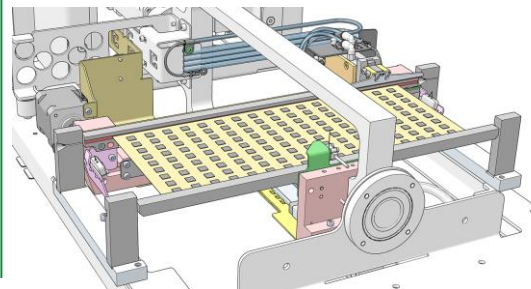
- Zero defect
- Advanced vision (upto 30 inspections)
- Individual package marking
- High speed reject punching
- Highest UPH (upto 220 str/min)
- Flexibility by common modules

New Developments 2022

Focus on power packages

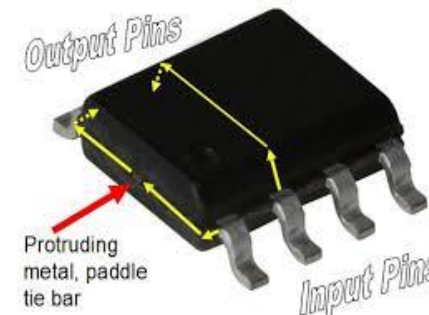
Leadframe flipping

Top and bottom
Laser marking and inspection



Tiebar-less handling

Package reliability



Low stress cutting

Preventing micro cracks

TN35.11.20 LSP (low Stress Profile) Punch angle shape



Besi's Plating and Wet Processing Systems are Industry Standards for Leadframe Plating



> 820 Systems Shipped



Leadframe plating line

Target Markets

- **Server** : System in packages
- **Automotive** : SOIC and TSOP packages
- **Solar** : TOPcon and Heterojunction cells



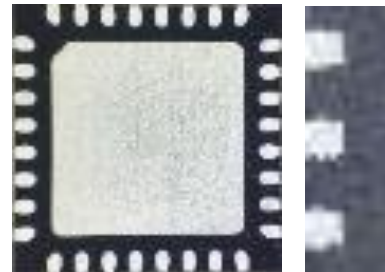
Key competitive advantages

- Market leader for leadframe plating
- Very low chemical consumption
- High resolution selective plating saving precious metals
- Best-in-class environmental footprint
- Lowest Cost-of-Ownership
- High productivity per m²

New Developments 2022

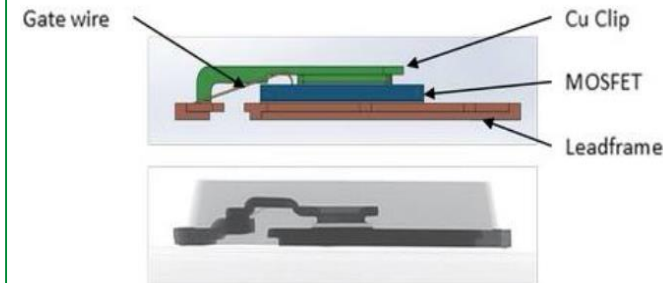
Wettable Flank QFN

- Plating of QFN after full cut saw
- Deburr process for step cut saw
- Improved reliability for automotive



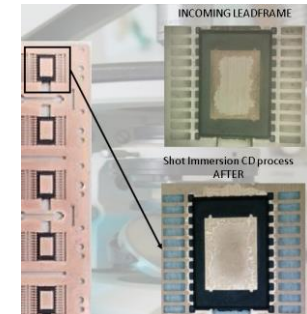
Flux Cleaning - Clip Attach

- Pre-mold cleaning for power applications
- Improved yield and quality for automotive



Short Chemical Deflash

- Post-mold removal of residual resins
- Inline with plating; 2 min process time



Packaging and Plating Growth Opportunities

Substrate AMS-LM



Wafer Molding FML



Leadframe Molding



Trim & Form FCL



Singulation FSL



Plating EPL

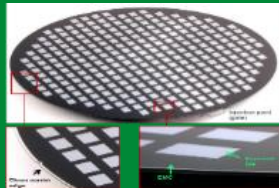


Sip Packages



- Wearables
- 5G mmWave
- Mems

Wafer molding



- Hybrid bonding
- Antenna in Chip

High power



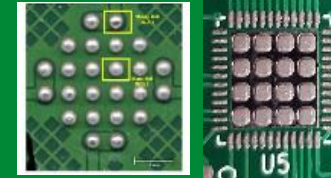
- Autonomous driving
- Electric motors

Industry 4.0



- Zero Defects
- Factory automation

RF Device

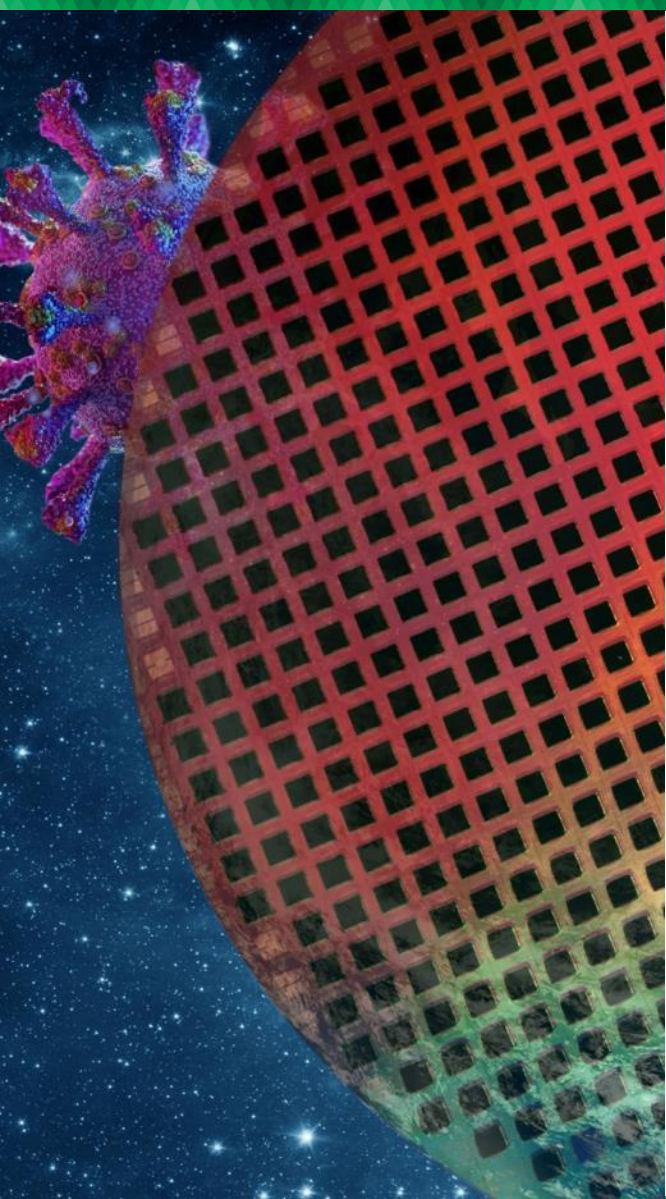


- RF Devices
- QFN power packages

Automotive & Industrial



- Autonomous driving
- Electric motors



VIII. Q&A

**Assembly market
ever more critical in
semiconductor value
chain**

**Disciplined strategic
focus has created an
industry leader**

**Long term secular
trends drive
advanced packaging
growth**

**Wafer level assembly
new growth
opportunity**

**Market presence has
grown via key IDMs,
supply chains and
partners**

**Tech leadership and
scalability result in
superior financial
returns**

**Commitment to
sustainable growth
and fighting climate
change**

**Attractive capital
allocation policy**