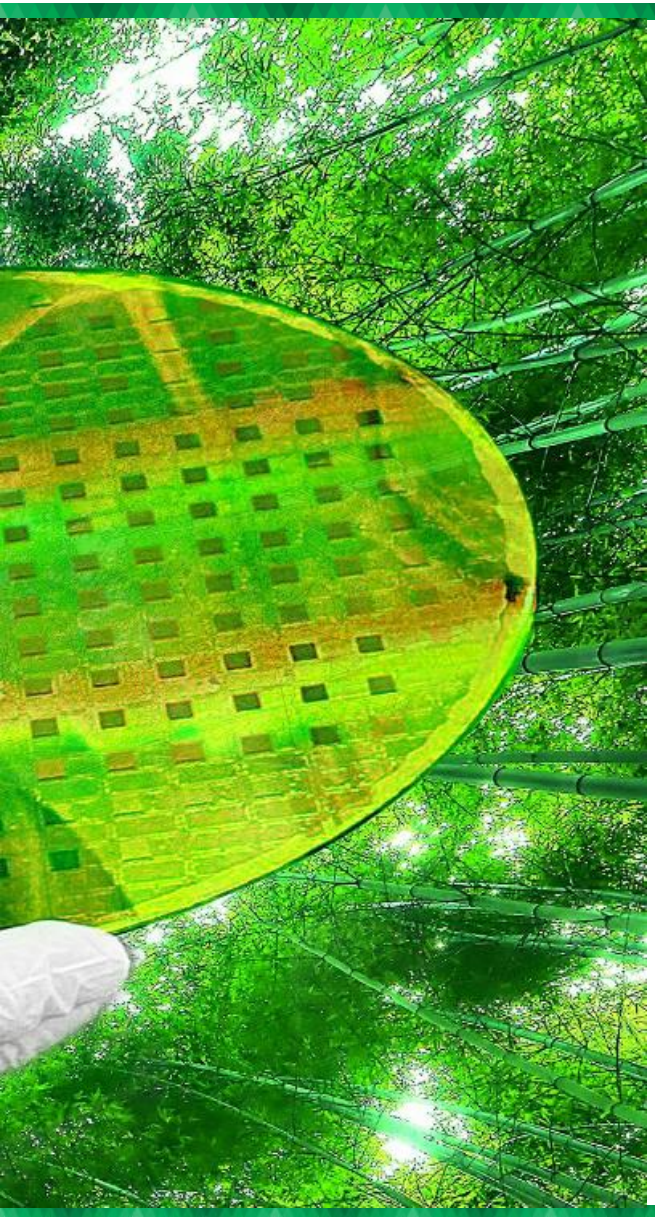


CAPITAL MARKETS DAY PRESENTATION

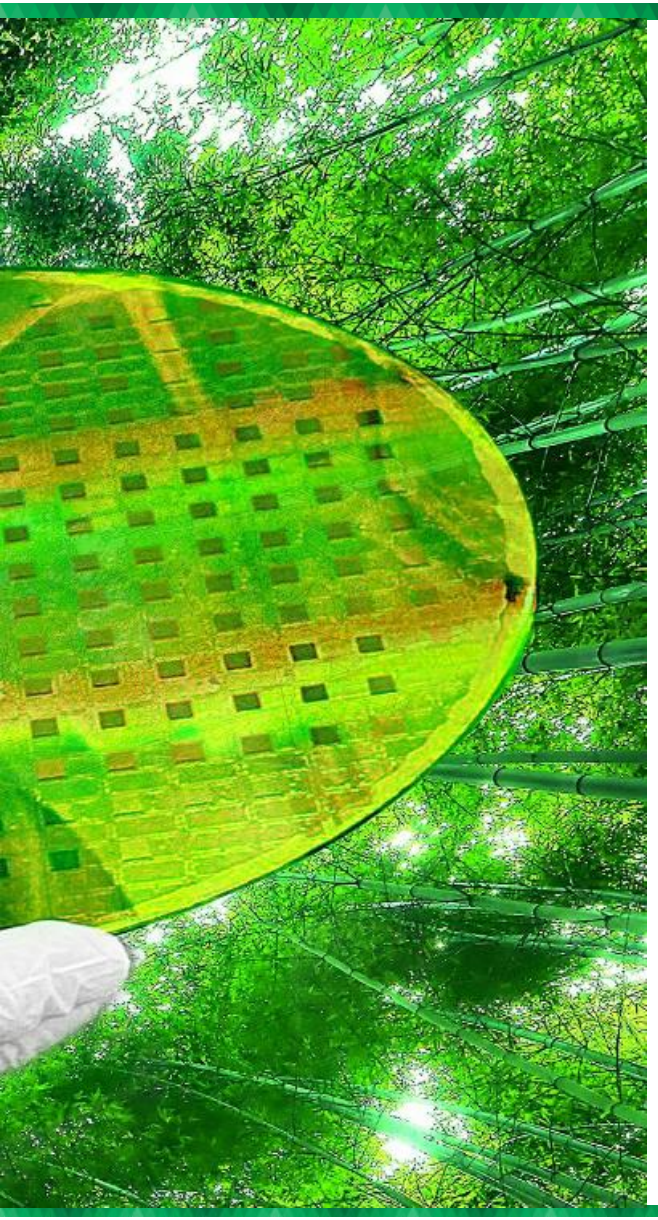
June 6, 2023

Safe Harbor Statement

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward-looking statements, which are found in various places throughout the presentation, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward looking statements, although not all forward-looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward-looking statements. While these forward looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 pandemic and measures taken to contain the outbreak, and the associated adverse impacts on the global economy, financial markets, global supply chains and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; consolidation activity and industry alliances in the semiconductor industry that may result in further increased customer concentration, inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, conflict minerals regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region where we have a substantial portion of our production facilities, potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel, including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers as a result of the COVID-19 pandemic; those additional risk factors set forth in Besi's annual report for the year ended December 31, 2022 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.

Agenda

I.	Strategic Overview	Richard Blickman
II.	Market Trends	Chris Scanlan
III.	Wafer Level Assembly	Peter Wiedner
IV.	Mainstream Die Attach	Christoph Scheiring
V.	Packaging	Jeroen Kleijburg
VI.	Plating	Bart Berenbak
VII.	Q&A	Besi Team



I. STRATEGIC OVERVIEW
Richard Blickman
CEO

CEO Summary

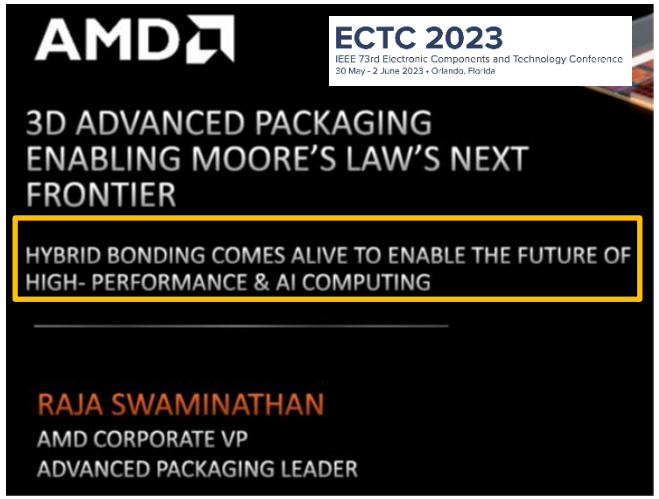
Hybrid Bonding Continues to Gain Traction

- Hybrid bonding not a question of if, but when, and how large the opportunity
  - AMD/TSMC achieved full commercial production for initial devices
  - Adoption increasing by industry and development community. Better than anticipated
  - Path won't be straight line but in increments
  - Integrated hybrid bonding production lines now a reality
  - Volume orders anticipated in 2024-2026 period
- TCB C2W also becoming more important factor in customer road maps

Strong Secular Drivers Intact to Advance Long-Term Growth

- Generative AI further accelerates move to digital society and smart everything
- Extension of Moore's law requires increased high-end assembly investment
  - Heterogeneous integration in 2.5/3D structures for HPC, HBM, Mobile and Automotive
- New investment required for onshoring capacity to Europe, US, Japan and SE Asia
- Mobile driven by increased 5G deployment and advanced camera modules
- EV drives automotive growth

Chiplets/Hybrid Bonding Increasingly in Focus



McKinsey & Company

Advanced chip packaging: How manufacturers can play to win

May 24, 2023 | Article

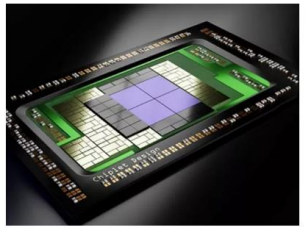
In terms of manufacturing, the two key technological capabilities manufacturers need to master for 2.5-D and 3-D packaging are, respectively, interposers and hybrid bonding. For 2.5-D, manufacturers must be able to handle emerging interposer solutions using novel materials and manufacturing methodologies, including silicon, RDL, and glass. For 3-D, the latest technology, hybrid bonding, requires chemical mechanical planarization to polish various substances with equal flatness and prevent dishing, as well as high interconnect accuracy through disk-to-wafer capabilities in both equipment and know-how.

February 14, 2023

As Chiplets Go Mainstream, Chip Industry Players Collaborate to Overcome New Development Challenges

SEMICON TAIWAN

By Ashley Huang

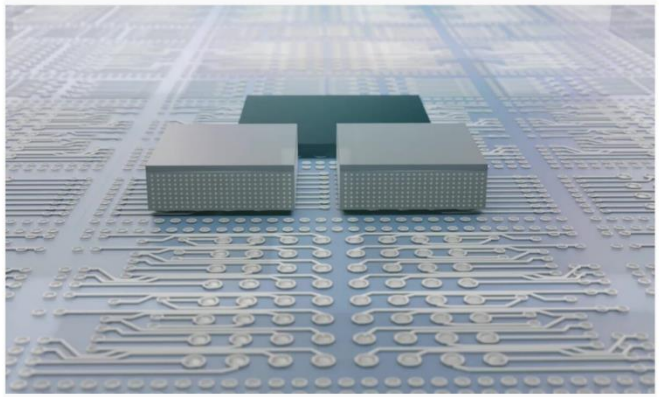


The semiconductor industry is building a comprehensive chiplet ecosystem to seize on the advantages of the devices over traditional monolithic system-on-chips (SoCs) such as improved performance, lower power consumption, and greater design flexibility. With heterogeneous integration (HI) presenting significant challenges, collaboration to fulfill the

Hybrid Bonding takes Heterogeneous Integration to the Next Level

3D In-Depth, Processes and Technology
May 22, 2023 · By Stephen Hiebert · heterogeneous integration, KLA

3DInCites



Applied Materials Convenes Leaders from Industry, Academia and Government at "Summit to Advance Semiconductor Leadership"

May 22, 2023 18:42 ET| Source: Applied Materials, Inc. Follow

CEO Summary - Continued

Strong Performance in Current Downturn

- Revenue, orders and operating profit up 44.7%, 66.5% and 82.7% vs. last cycle
  - Peer leading gross and operating margins up 5.6 and 8.1 points
- Addressable market share increased in key die attach and packaging markets
- Record capital allocation of € 416.3 million in 2022. € 347.8 million YTD 2023

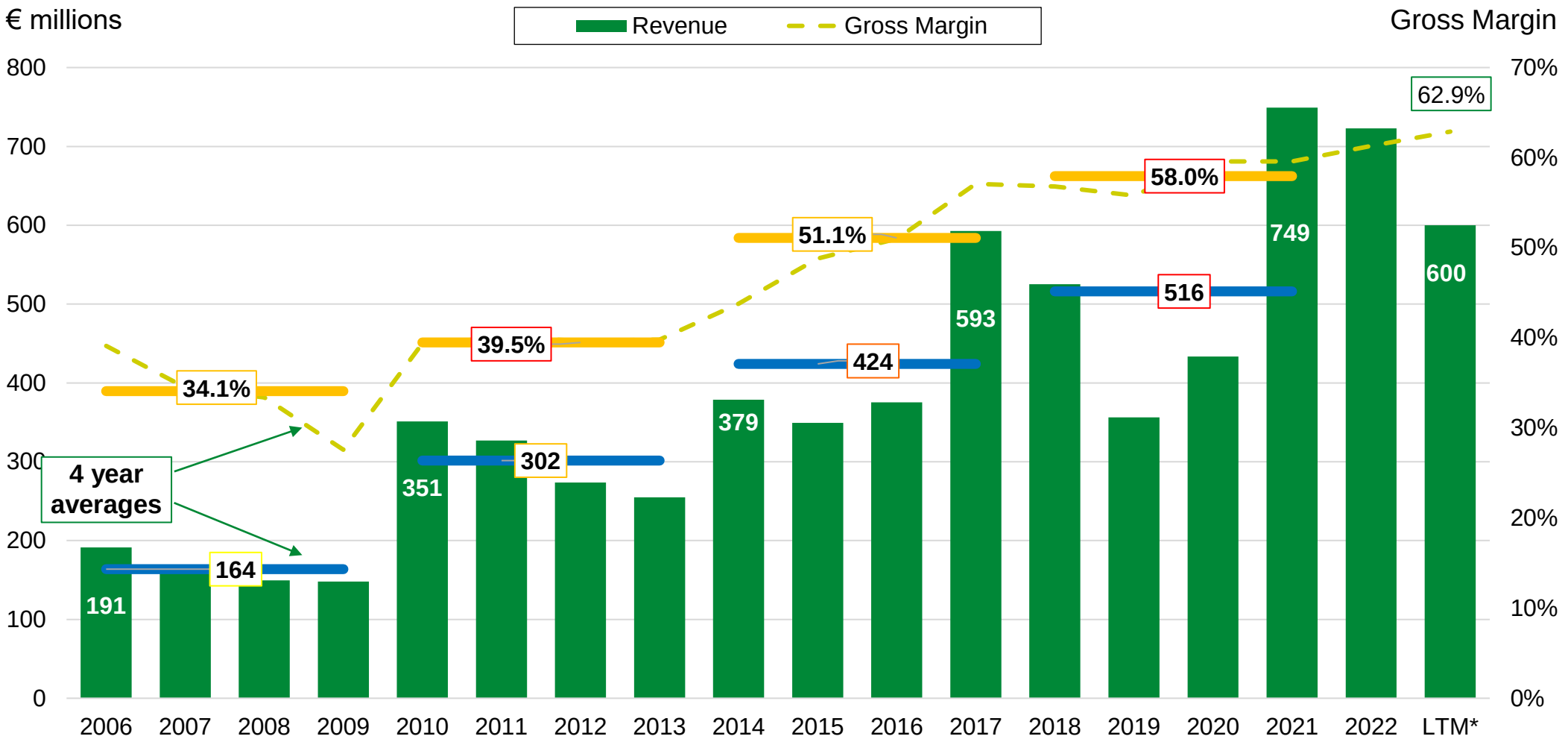
Many Potential Variables for H2-23

- Typical assembly cycle would indicate new order upturn Q3/Q4
- China 7 Quarters into downcycle
- Wildcards: Direction of inflation and US/China GDP, Geopolitical tensions

Well Positioned for Next Industry Upturn

- Best in class assembly portfolio
  - First generation wafer level assembly systems introduced
- Market moving to sweet spot of core technological competencies
- Business model revenue targets intact. Capacity and personnel in place
- Expansion in US, Vietnam and Taiwan in alignment with customer road maps

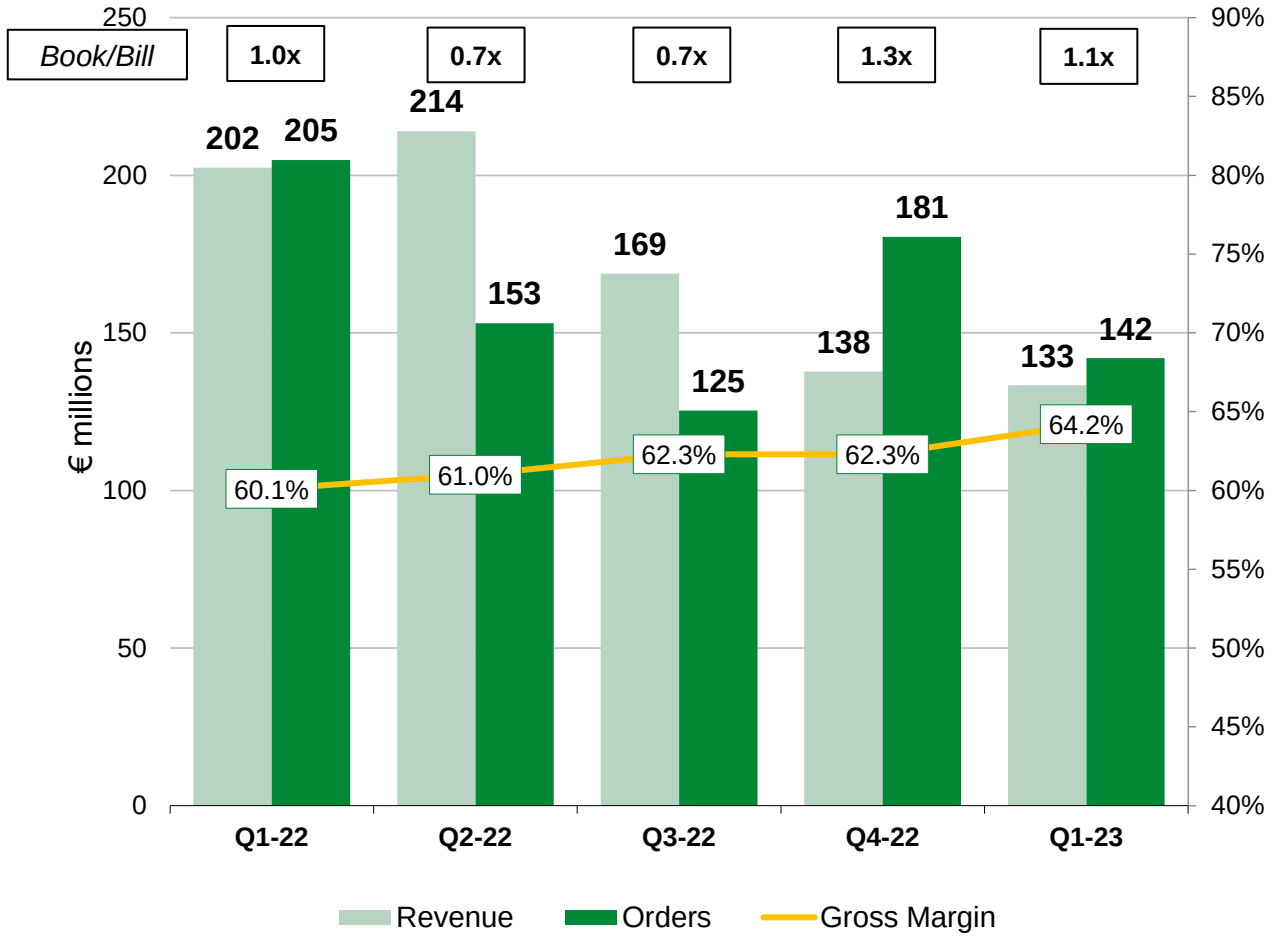
Strong Through Cycle Revenue and Gross Margin Development



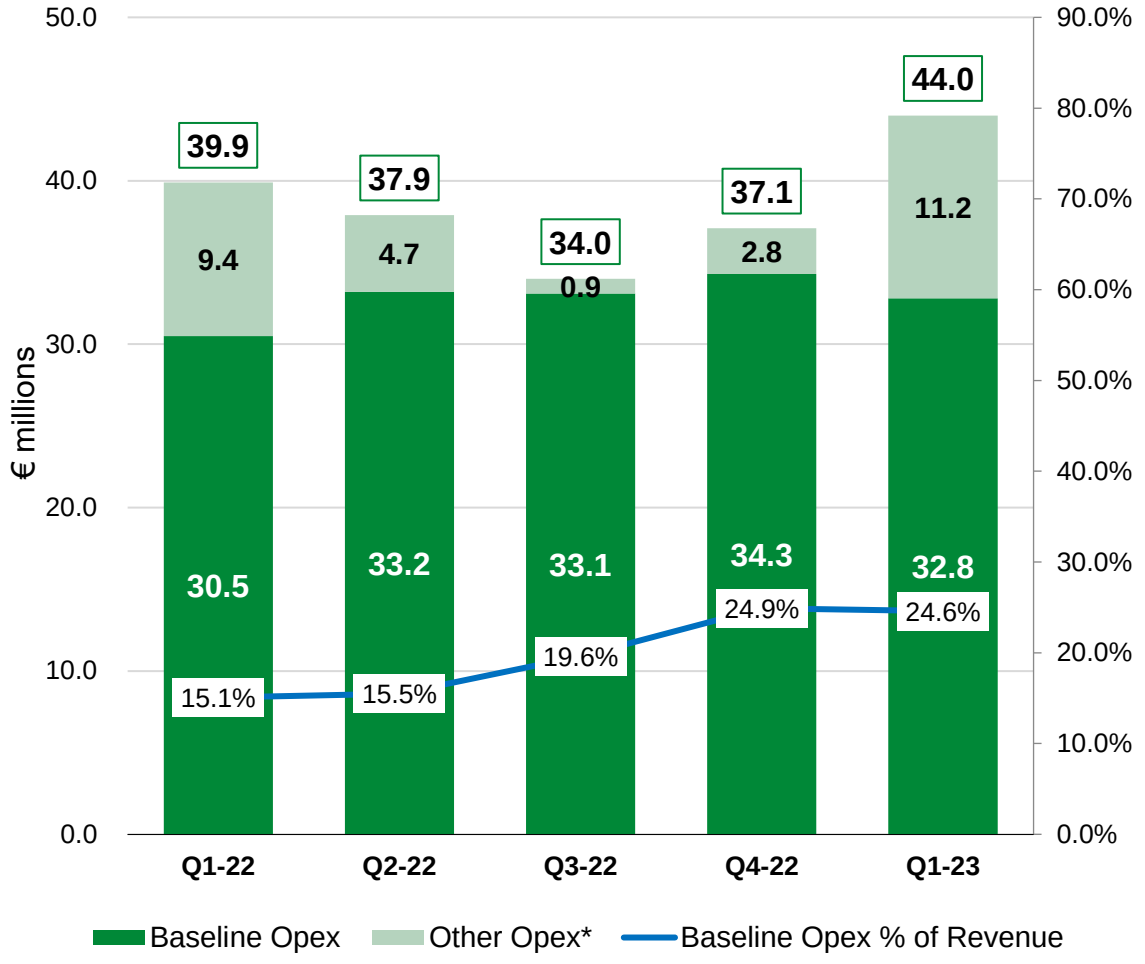
* LTM including midpoint of guidance for Q2-23.

Attractive Profit Efficiency Maintained In Downturn
Strategic Initiatives Keep Opex in Check Despite Increased R&D

Revenue, Orders and Gross Margin



Baseline Operating Expenses



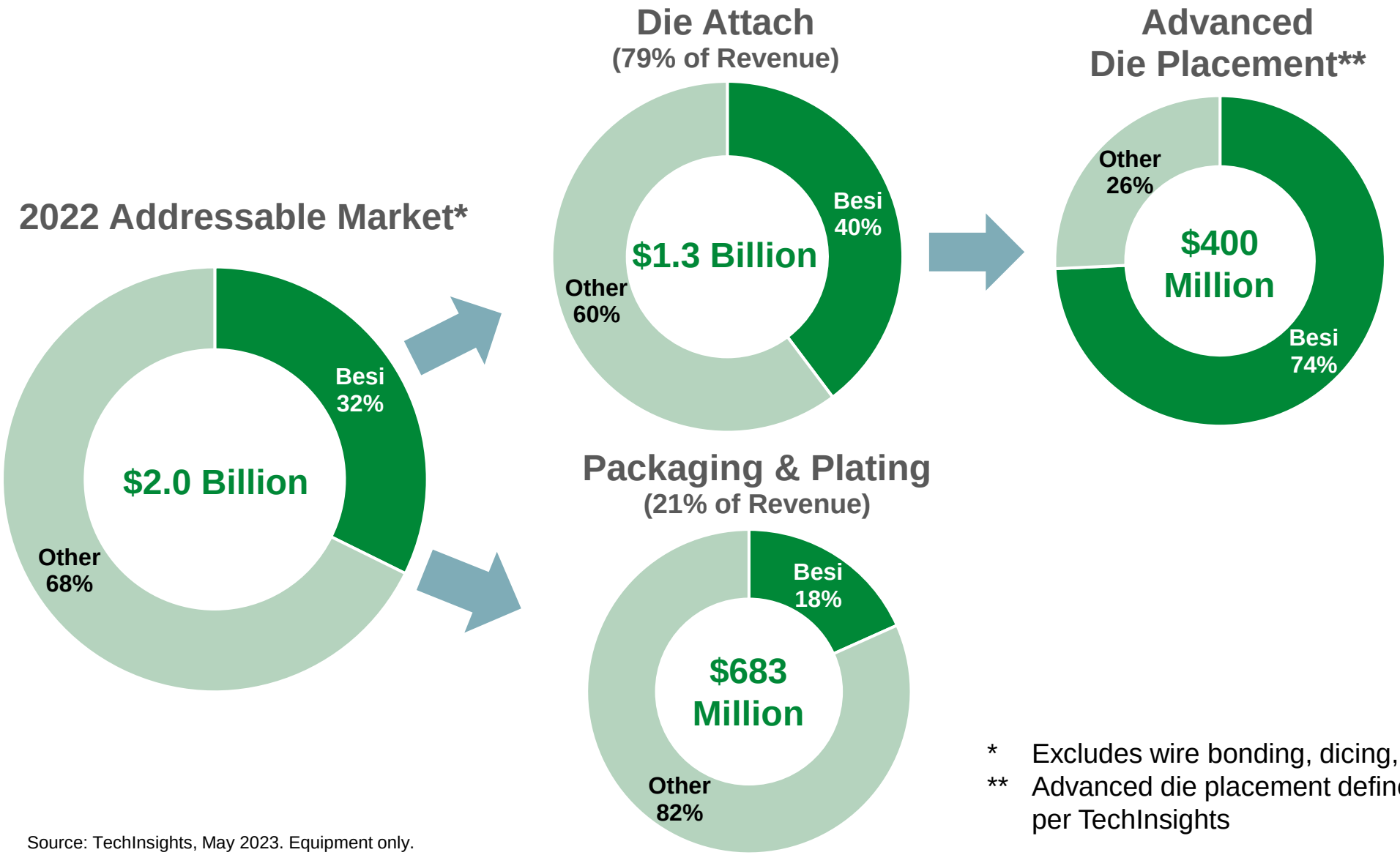
* Other Opex includes both short-term and long-term incentive compensation, restructuring costs, net R&D capitalization/amortization and certain one-time items.

Besi Addressable Market Share Increasing Particularly in Key Die Attach Markets

	2016	2018	2020	2021	2022	Δ '22/'21	Δ '22/'16
Assembly Market ($MM)	3,587	4,542	3,916	6,597	**5,540**	-16.0%	+54.5%
Besi Market Share	9.9%	11.2%	10.5%	11.7%	**11.5%**	**-0.2pts**	**+1.6pts**
Addressable Market ($MM)	1,507	1,859	1,439	2,444	**1,966**	-19.6%	+30.5%
Besi Market Share	23.7%	27.3%	28.5%	31.7%	**32.3%**	**+0.6pts**	**+8.6pts**
Die Attach	30.4%	33.2%	35.4%	39.4%	**39.7%**	**+0.3pts**	**+9.3pts**
Packaging & Plating	13.6%	17.0%	15.3%	15.7%	**18.3%**	**+2.6pts**	**+4.7pts**
% of Besi Revenue	**2016**	**2018**	**2020**	**2021**	**2022**	**Δ '22/'21**	**Δ '22/'16**
Die Attach	75%	76%	82%	82%	**79%**	-3pts	**+4pts**
Packaging & Plating	25%	24%	18%	18%	**21%**	**+3pts**	-4pts

Source: TechInsights, May 2023

Leader in Addressable Market, Die Attach Market and Advanced Die Placement



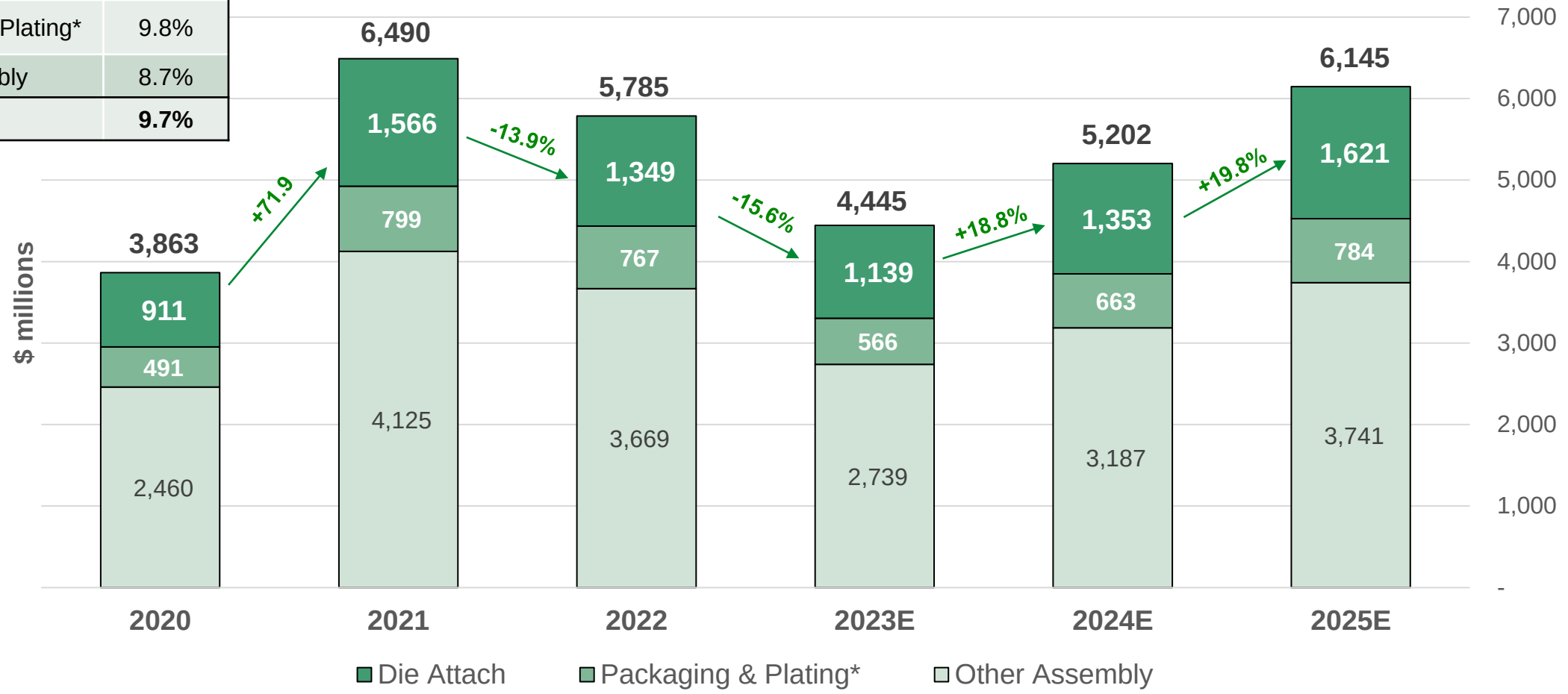
Source: TechInsights, May 2023. Equipment only.

* Excludes wire bonding, dicing, and other.

** Advanced die placement defined as < 7 micron accuracy per TechInsights

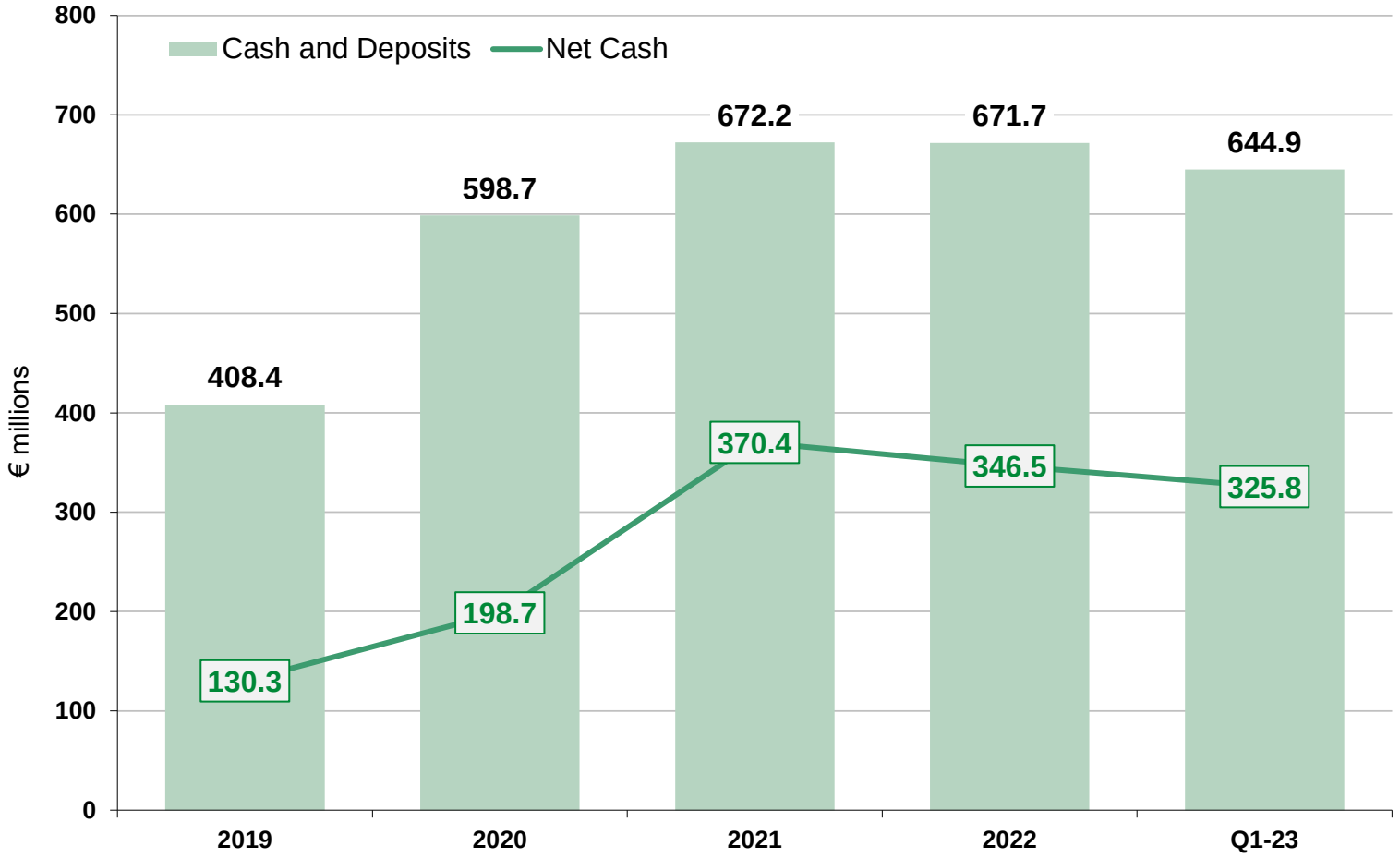
Growth Expected to Favor Besi's Product Portfolio, Particularly Die Attach

CAGR (2020-2025)	
Die Attach	**12.2%**
Packaging & Plating*	9.8%
Other Assembly	8.7%
Total	**9.7%**



Source: **TechInsights, March 2023. Addressable market revenue excludes hybrid bonding contribution**.
* Packaging & Plating includes only Besi's addressable segments. Non-addressable reported in other assembly market.

Strong Liquidity Position Maintained to Finance Future Growth



Strong liquidity base consisting of cash and deposits of € 644.9 million

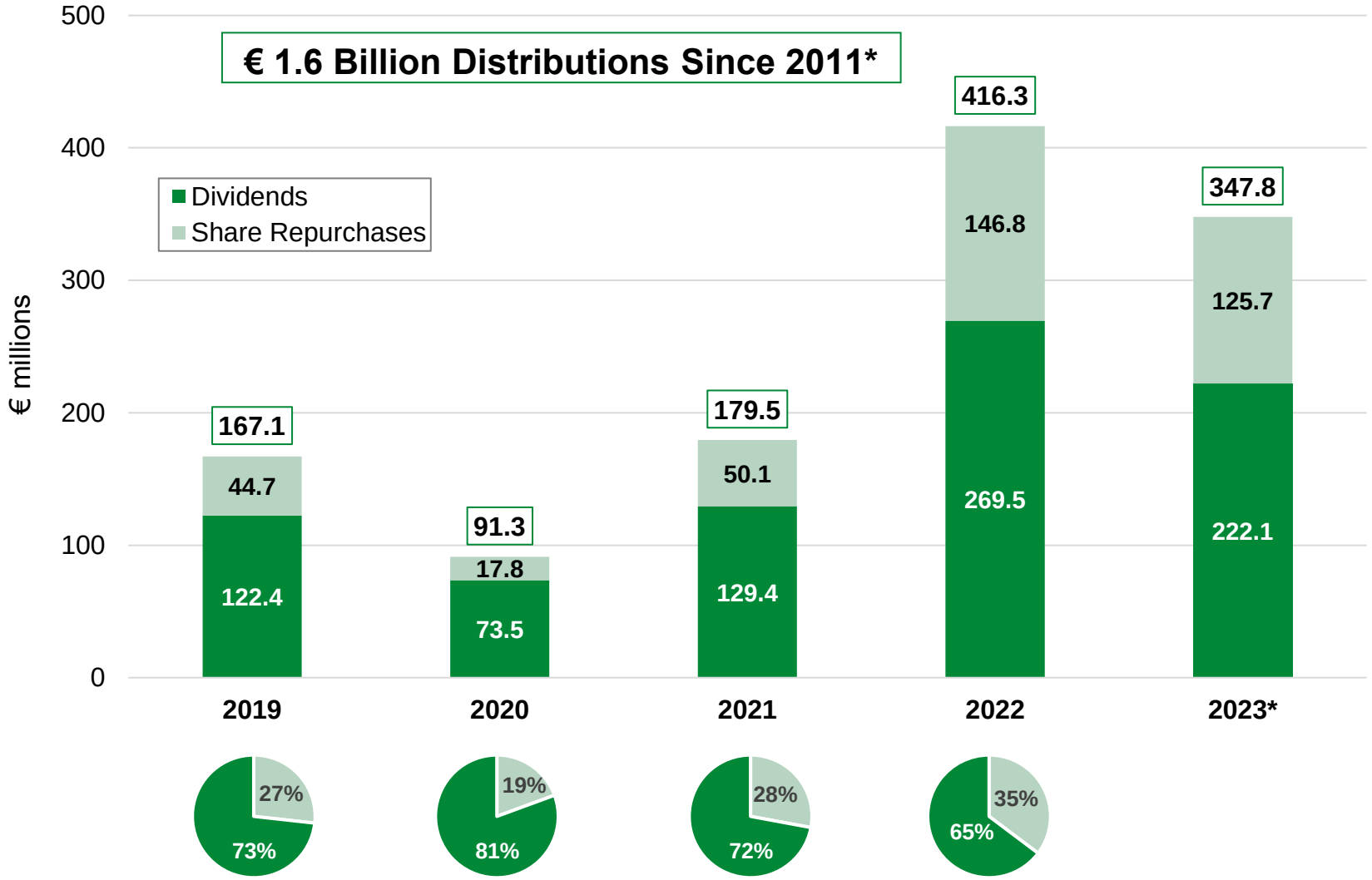
Net cash of € 325.8 million equals 54% of LTM revenue

- Significantly in excess of 20% threshold

Convertible Notes have decreased to € 336.1 million at May 31, 2023

- 2024 Notes reduced to € 10.5 million
- 2023 Notes reduced to € 0.6 million

Capital Allocation Increasing to Shareholders



~ € 320 million capital allocation YTD-23

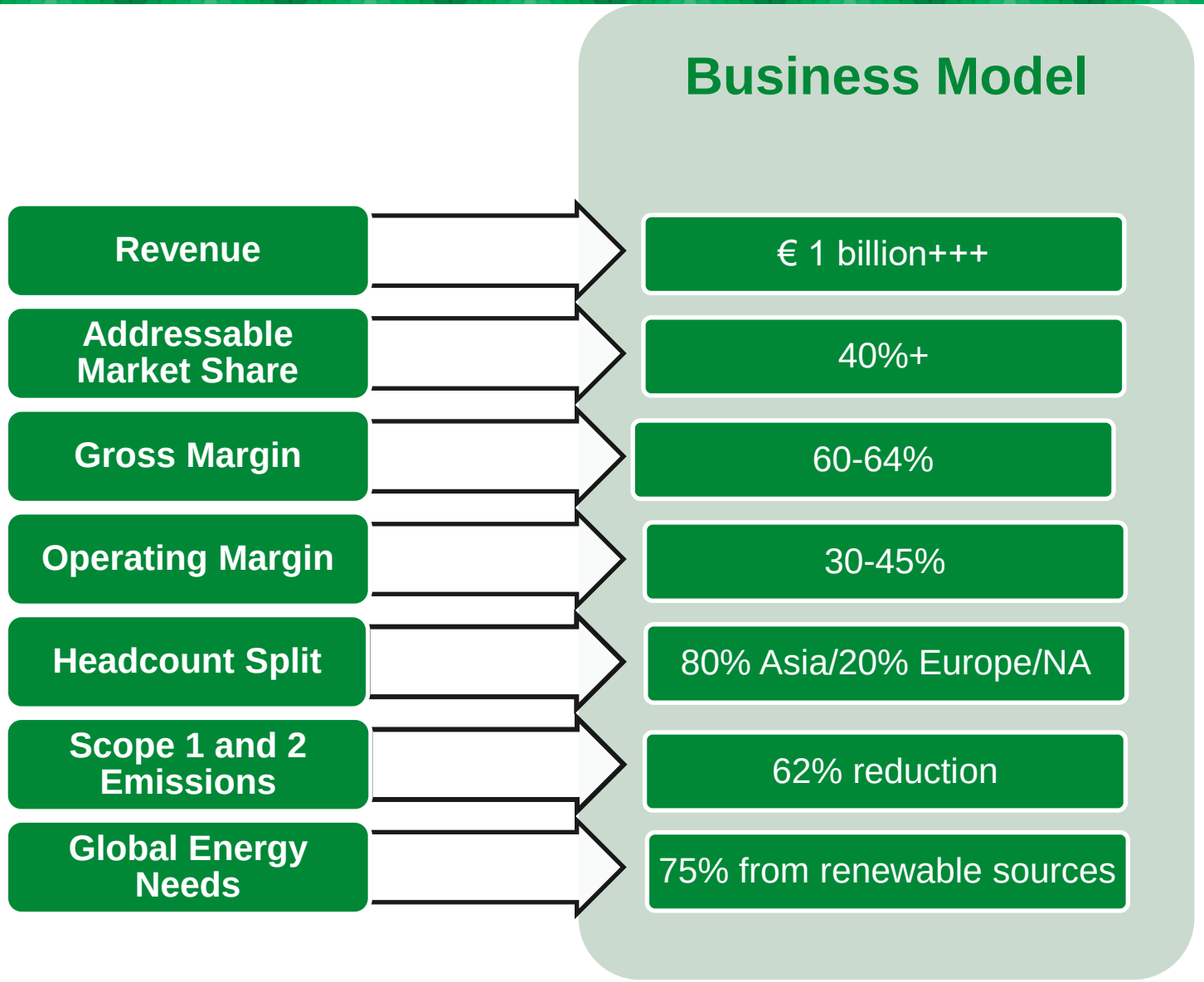
€ 300 million share buyback program ~75% completed :

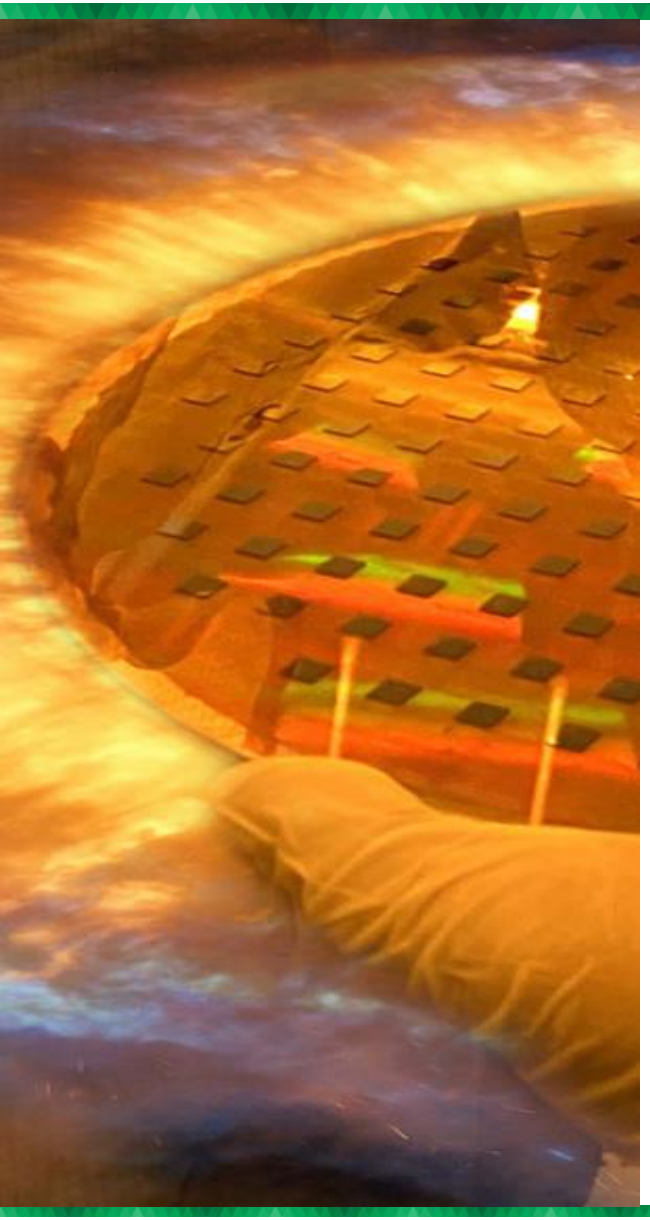
- ~ € 75 million per quarter
- ~3.5 million shares purchased through May-23 for € 222.1 million
- Expected completion: October 2023

Fully diluted shares reduced by ~2.0 million since 1/1/2022

* Includes dividend of € 2.85 per share for 2022 and share repurchases through May 31, 2023

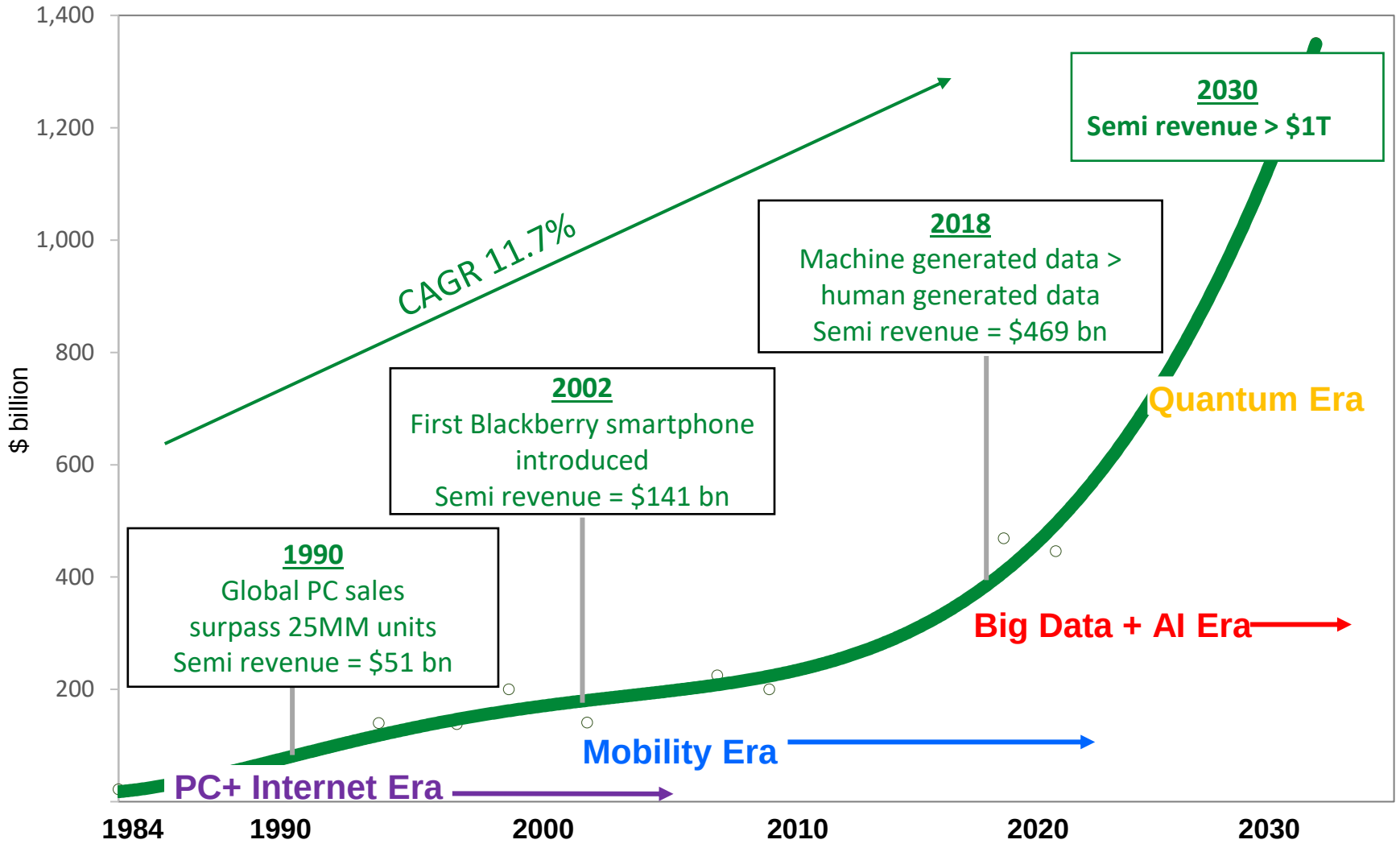
Business Model





II. MARKET TRENDS
Chris Scanlan
SVP Technology

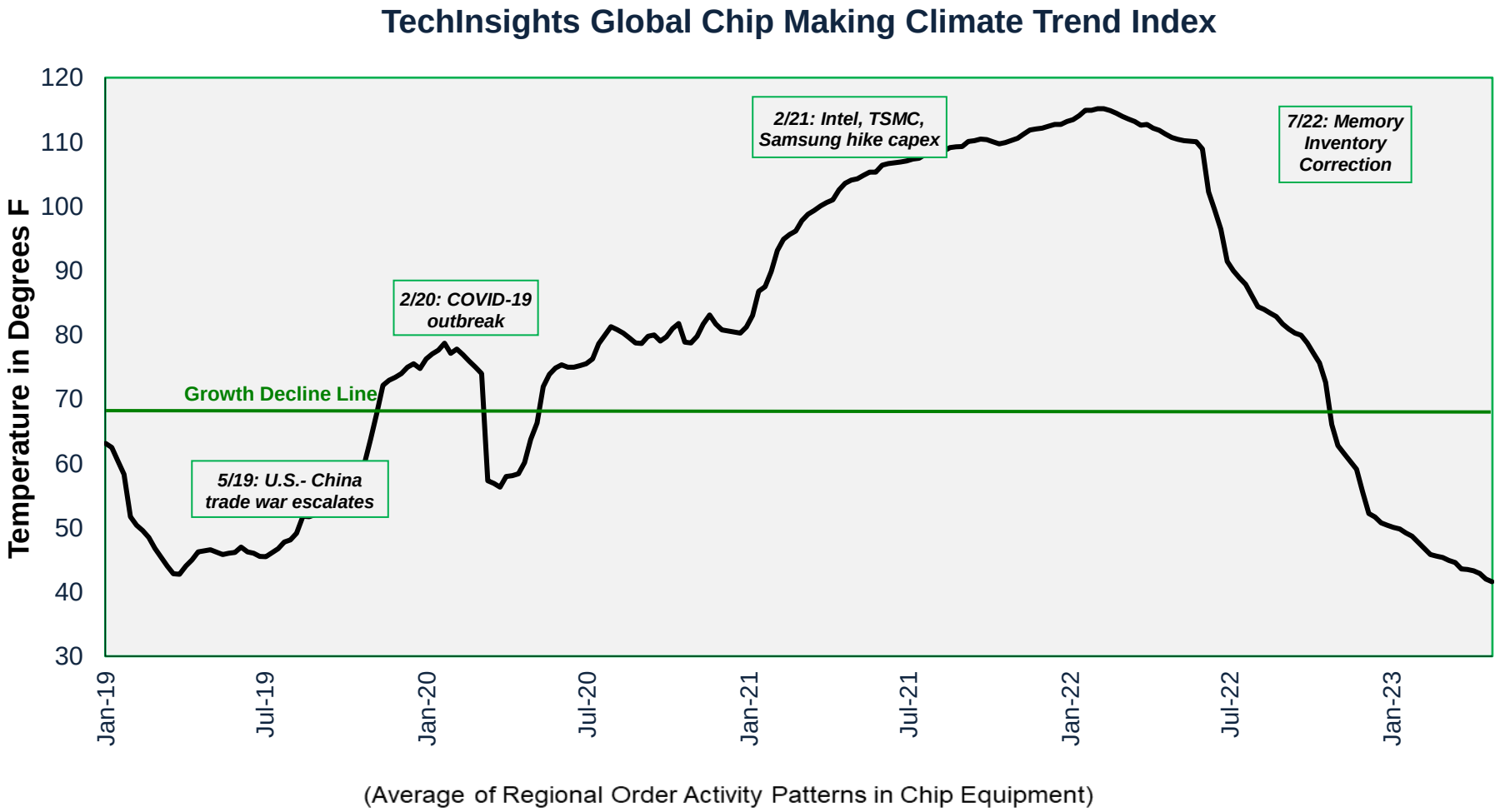
Long-Term Semiconductor Demand Growth Continues



Data source: SEMI 2022

- Market required ~50 years to reach $500 billion in sales
- Estimates call for > $1 trillion in sales within next 10 years

Industry Downturn Continues in 2023



Source: TechInsights, May 2023

Semi Capex Expected to Decline 17% in 2023

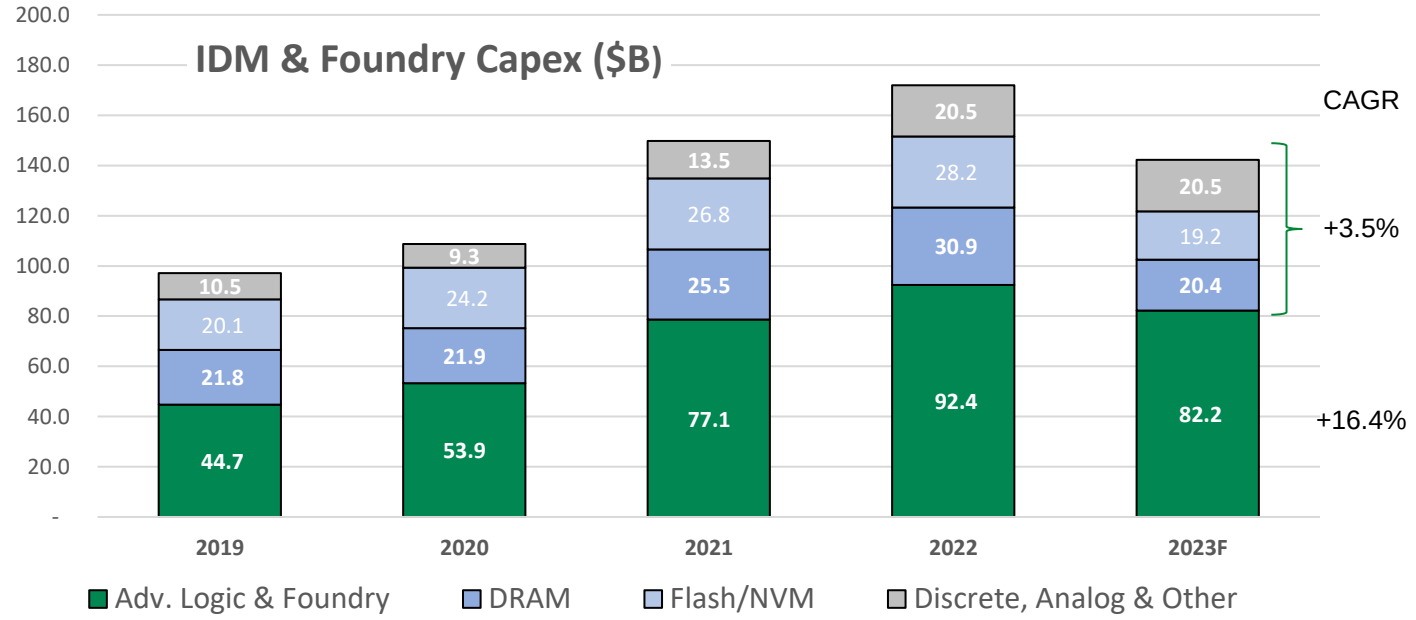
TOP 20 CAPEX SPENDERS

(Capital expenditures by company, $M, ranked by 2023 Capex)

	2019	2020	2021	2022	2023
TSMC	14.9	17.2	30.0	36.3	34.9
Samsung	19.3	28.1	38.0	36.6	33.3
Intel	16.2	14.3	18.7	23.7	16.2
Micron	8.6	8.8	10.2	11.2	7.5
SK hynix	12.0	8.4	10.9	13.9	6.9
SMIC	2.0	5.7	4.5	6.4	6.2
STMicroelectronics	1.2	1.3	1.8	3.5	4.0
Infineon	1.3	1.1	1.6	2.3	3.2
Sony	2.3	2.4	2.6	2.9	3.1
UMC	0.6	1.0	1.8	2.7	3.0
GLOBALFOUNDRIES	0.6	0.6	1.8	3.1	2.3
Texas Instruments	0.8	0.6	2.5	2.8	2.0
KIOXIA	1.3	1.5	3.5	2.1	1.8
Western Digital	1.6	2.0	1.9	1.5	1.4
CXMT	1.4	2.5	2.9	2.6	1.4
ON Semiconductor	0.5	0.4	0.4	1.0	1.3
XMC/YMTC	2.1	2.9	3.1	3.0	1.3
NXP	0.5	0.4	0.8	1.1	1.0
Analog Devices	0.3	0.2	0.3	0.7	0.9
Renesas	0.1	0.2	0.8	1.7	0.9
Top 20 Total	87.6	99.5	138.3	159.2	132.6
Growth Rate		*13.5%*	*39.0%*	*15.1%*	*-16.7%*

Top 3 (% of Total)	**58%**	**60%**	**63%**	**61%**	**64%**
Top 5 (% of Total)	**81%**	**77%**	**78%**	**76%**	**75%**

Source: Tech Insights, May 2023



2023E Semi capex for top 20 producers to decline 17% to € 132.6 billion

- 86% of decrease represented by top 5 spenders
- Mostly for memory applications

Growth in Advanced Logic and Foundry has significantly exceeded memory spending in recent years

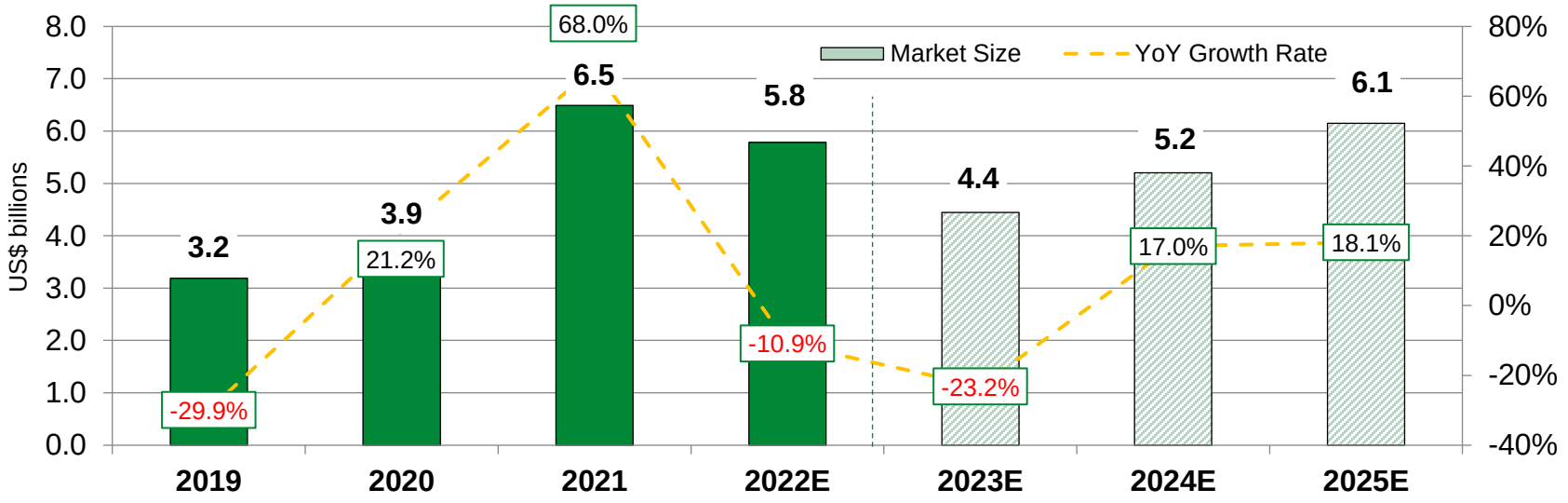
- CAGR of 16.4% 2019-2023 vs. DRAM/Flash/NVM CAGR 3.5%
  - Represents ~58% of total WFE spending in 2023

Long Term Investment Continues, Aided by Government Support
$82.6 Billion Direct and $159.2 Billion Indirect Spending/Annum Planned

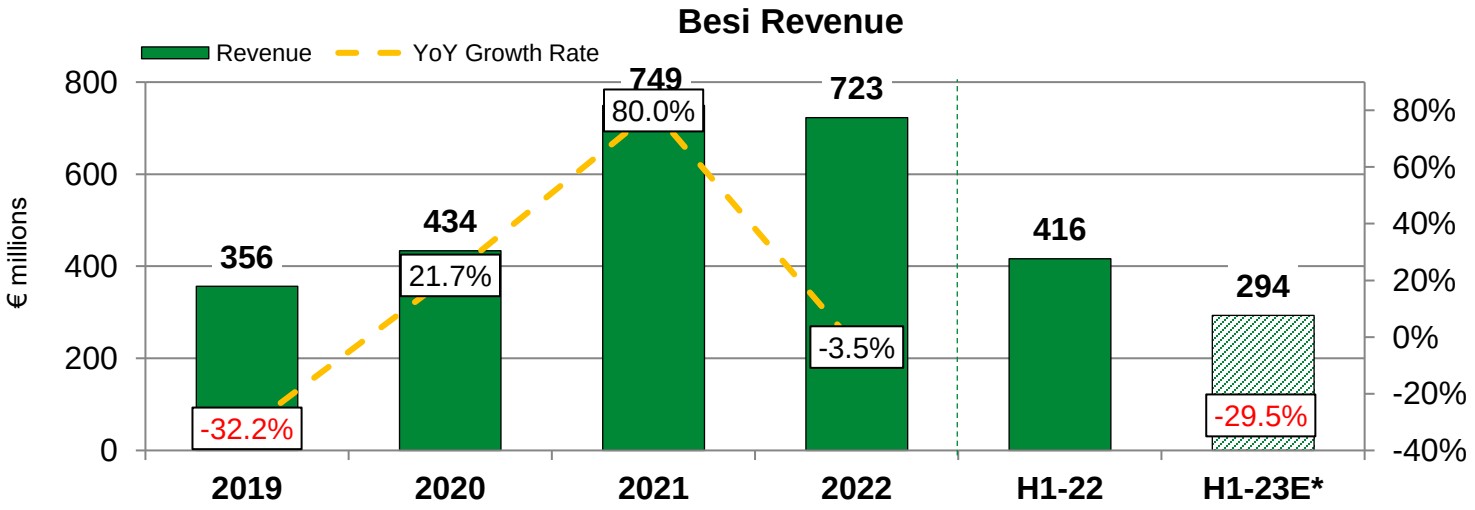
Besi

TechInsights May 2023	Date	Amount $	Timing	$ p.a.	Location	Purpose
Direct Investments						
TSMC	Dec 2022	**40.0B**	5 years (2027)	**8.0B**	AZ	New 4nm fab (late 2024) & 3nm fab (2026)
TSMC	Dec 2022	**60.0B**	4 years (2026)	**15.0B**	TW	New fabs in Taiwan
Micron	Oct 2022	**100.0B**	~20 years (~2042)	**5.0B**	NY	New DRAM megafab
Micron	Sep 2022	**15.0B**	3 years (2025)	**5.0B**	ID	New leading edge fab
Intel	Sep 2021	**20.0B**	6 years (2027)	**3.3B**	AZ	2 new fabs <7nm
Intel	Sep 2022	**20.0B**	5 years (2027)	**4.0B**	OH	2 new fabs leading edge
GLOBALFOUNDRIES	July 2022	**8.0B**	3 years (2025)	**2.7B**	NY	Expansions/adding capacity
Texas Instruments	May 2022	**30.0B**	8 years (2030)	**3.8B**	TX	New 4 fabs in Sherman, TX (1st fab 2026)
Texas Instruments	Feb 2023	**11.0B**	3 years (2026)	**3.7B**	UT	Second fab in Lehi, Utah
Samsung	Jul 2022	**192.0B**	20 Years (2042)	**10.0B**	US	11 new fabs in the US
Samsung	Mar 2023	**230.0B**	20 Years (2042)	**11.4B**	KO	5 new fabs in S. Korea
SK hynix	Sep 2022	**106.5B**	10 Years (2032)	**10.7B**	KO	Adv. Memory and capacity expansion
Indirect Investments						
Apple	Apr 2021	**430.0B**	5 years (2026)	**86.0B**	USA	Next-gen silicon, 5G innovation, data centers
Intel	Mar 2022	**€ 80.0B**	10 years (2032)	**€ 8.0 B**	EU	European Union/Semi Capacity
USA	May 2021	**52.0B**	5 years (2026)	**10.4B**	USA	Semi capacity and R&D
EU	Apr 2023	**€ 47.0B**	8 years (2030)	**€ 5.9B**	EU	European Chips Act
Korea	May 2021	**450.0B**	10 years (2032)	**45.0B**	KO	Semi manufacturing incentives
Japan (JASM)	May 2021	**8.6B**	3 years (2024E)	**2.9B**	JP	<20nm fab

Assembly Market Estimates Reduced for 2023 Rebound Forecast 2024-2025



Source: TechInsights, April 2023. Assembly equipment revenue excludes hybrid bonding contribution and service revenue.



* At midpoint of Q2-23 guidance

TechInsights now forecasts 23.2% downturn in 2023

- Versus -16.8% prior forecast
- Market decreases to $4.4 billion
- ~32% decrease from 2021 peak
- Rebound anticipated in 2024 and 2025

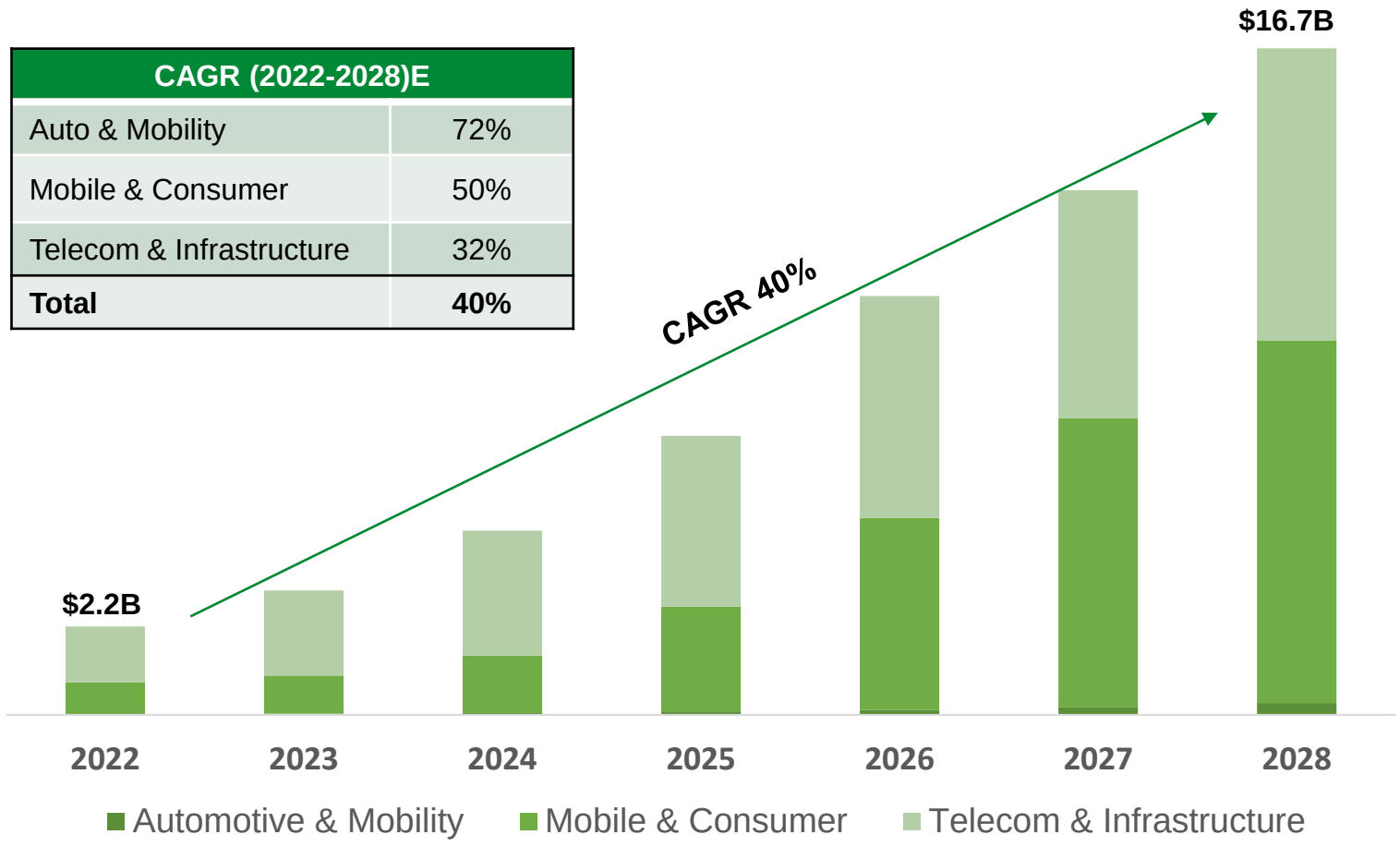
Strong secular fundamentals intact:

- AI, HPC, 5G/6G primary drivers
- Investment in new process technologies: hybrid bonding/CSP
- Onshoring new advanced packaging fabs

Advanced Packaging Revenue Growing Rapidly
Fastest Growing Assembly Segment

High End Performance Packaging Revenue ($B) by End Market

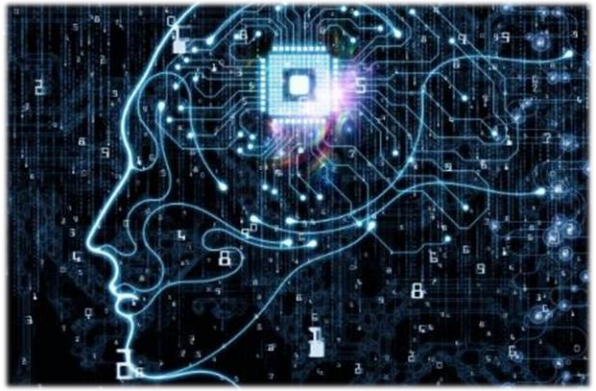
CAGR (2022-2028)E	
Auto & Mobility	72%
Mobile & Consumer	50%
Telecom & Infrastructure	32%
Total	**40%**



Data Source: Yole Development 2023

- Driven by multi-chip packaging and chiplet transition
- Requiring equipment with more advanced interconnect technology and higher accuracy
- Besi leading equipment supplier for AP die attach and molding

Besi Principal End User Markets/Drivers

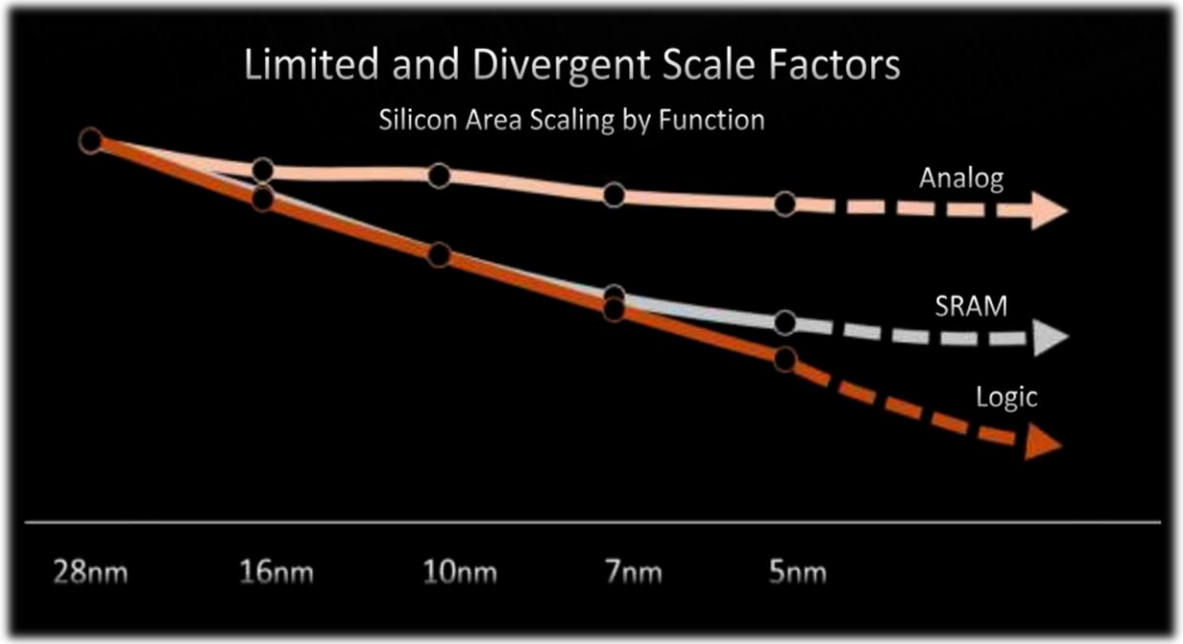
Mobile Internet (28%)	Computing (30%)	Automotive (16%)	Industrial/Other (9%)
			
Camera Innovation 5G Advanced → 6G Wearables On Device AI	Generative AI Datacenter Gaming Edge Computing	Vehicle Electrification Autonomous Driving Connectivity Infotainment	Clean Energy Smart Grid Industrial IoT Automation

%s Based on 2022 estimated revenue per end market application. Spares/service revenue was ~17% of 2022 revenue

Slowing of Moore's Law Drives Adoption of Chiplet Architectures and New Assembly Solutions

Problem

- Moore's Law slowing as data volumes grow exponentially and commercial applications expand
- Cost per transistor increasing
- Die area increasing even as node sizes reduce

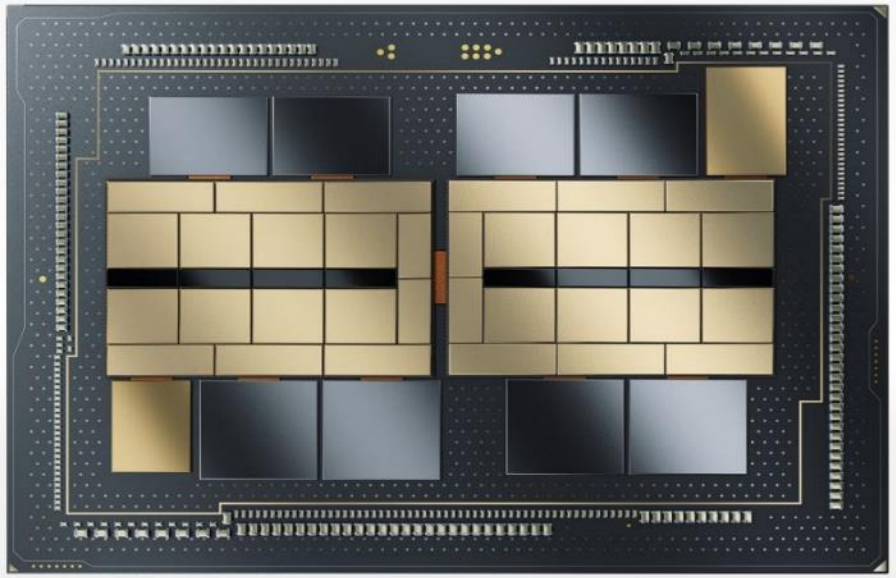


Source: AMD

Solution

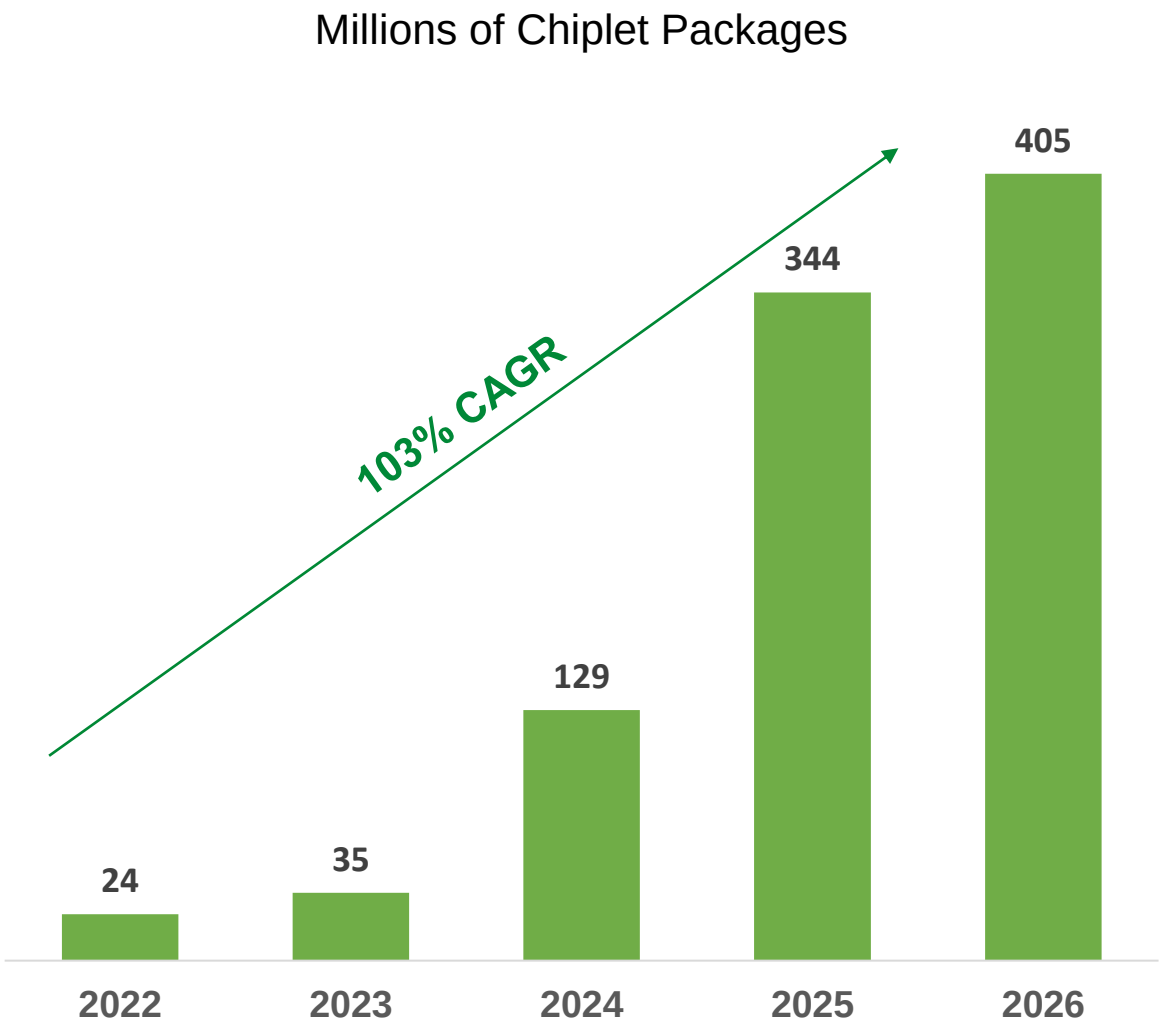
- Split SoC into multiple, smaller **chiplets**
- Optimize scale per function
- Connect chiplets within package utilizing hybrid bonding and C2W TCB

Intel's Ponte Vecchio: 47 Active Chiplets in One Package



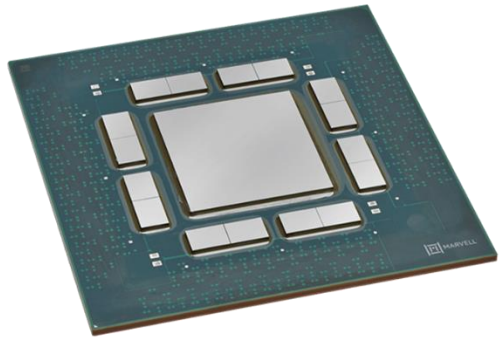
Source: Intel

Chiplet Adoption is Expected to Increase Rapidly Driven by Increasing Cost of Advanced Logic Nodes

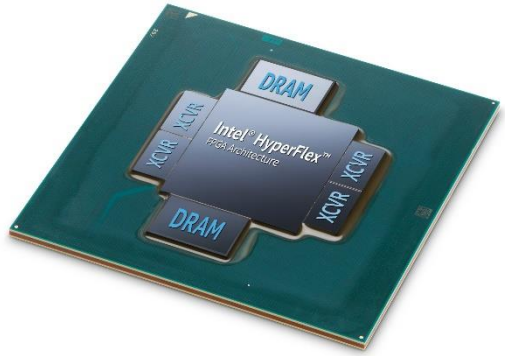


Data Source: Techsearch International

- **At 3nm node, economics will drive most applications to chiplets**
- Market forecast includes CPUs for server, desktop, laptop, GPU devices, network switch, AI / machine learning applications, future application processors

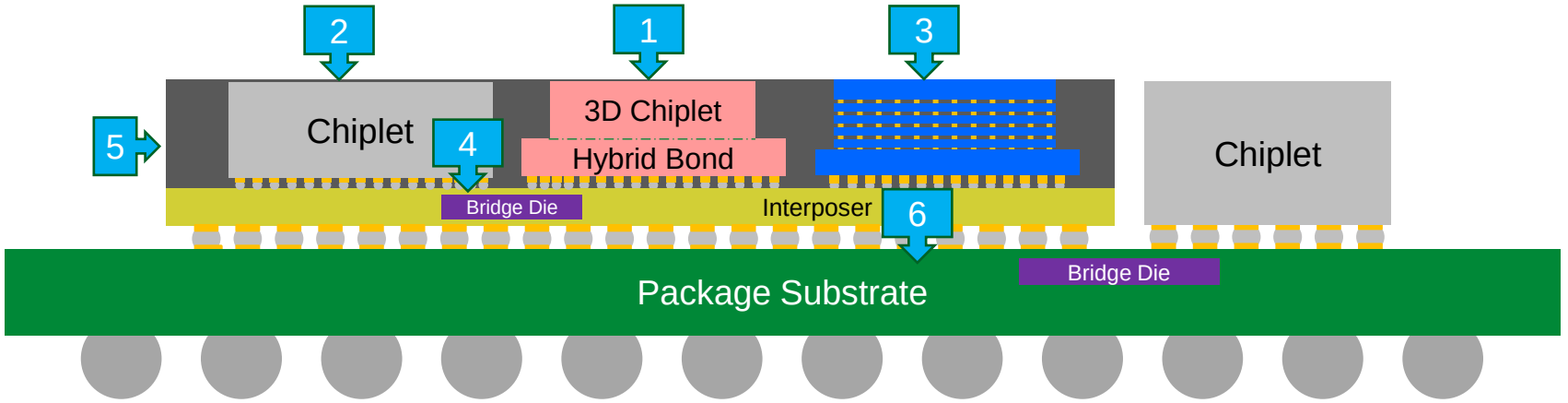


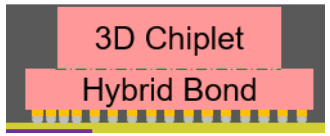
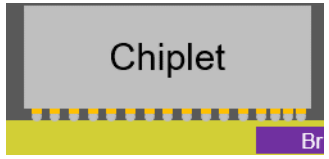
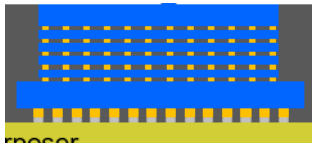
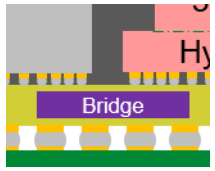
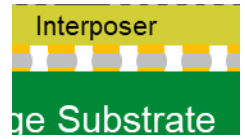
Marvell Data Center Switch
17 chiplets



Amazon Data Center CPU
7 active chiplets

New 3D Chiplet Structures Use Variety of Assembly Processes

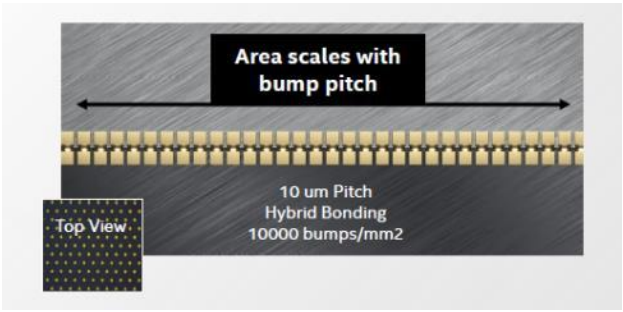


1	2	3	4	5	6
Hybrid Bonding	Chip to Wafer TCB	High Bandwidth Memory Stacking	Embedded Bridge Die Attach	Wafer Level Die Molding	HD Interposer to Substrate
					
8800 CHAMEO Ultra Plus	**9800 TC Next** C2W	**8800 CHAMEO** Ultra Plus **8800 TC Advanced**	**8800 Chameo** Ultra	**FML**	**2200 evo**

Hybrid Bonding Extends Moore's Law

Enables faster, more complex devices with submicron placement accuracy

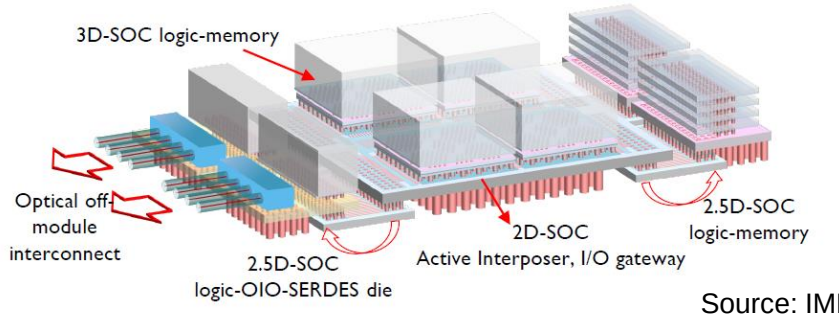
Direct Cu-Cu Interconnect in 3D



Source: Intel

1000x increase in contact density

Heterogeneous integration of chiplets



Source: IMEC

More transistors per package

New Chip Architectures

- Quasi-monolithic 3D
- Optimal use of nodes
- Customized designs
- Highly configurable

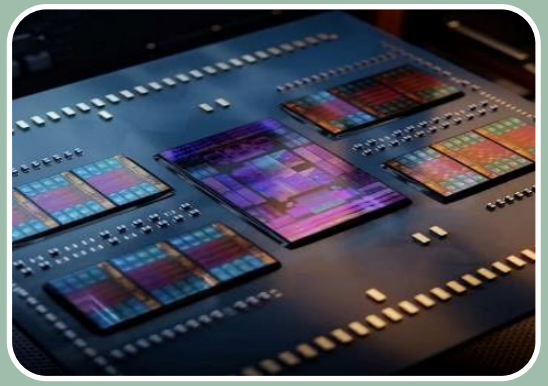
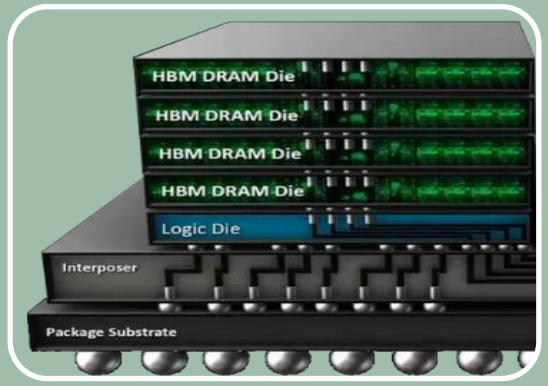
Increased Performance

- Highest compute power
- Increased data transfer
- Higher bandwidth
- Higher speed

Lower Cost of Ownership

- Higher die yield
- Lower energy per bit
- Lower cost per contact
- Lower heat dissipation

Applications Driving Hybrid Bonding Growth

High Performance Compute	Advanced Memory	Mobile	Sensors & Photonics
			
Unified Compute/Memory Core on Core	**Advanced Memory Stacking**	**Application Processors mmWave RF**	**Integrated Silicon Photonics**
AI Gaming Datacenters	HBM4 DRAM	Smartphones	Image Sensors AR/VR Display

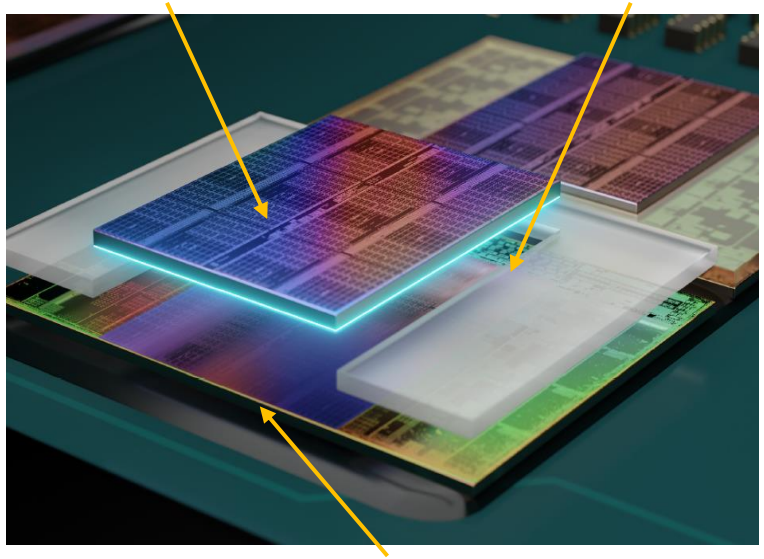
AMD Has Announced More Products Using Hybrid Bonding

Ryzen CCD with 3D V-Cache

- **CPU/memory for server and gaming**
- Additional 64 MB SRAM stacked atop Ryzen chiplets using hybrid bonding

SRAM die hybrid bonded to back of CCD chip

2 structural Si die hybrid bonded to CPU

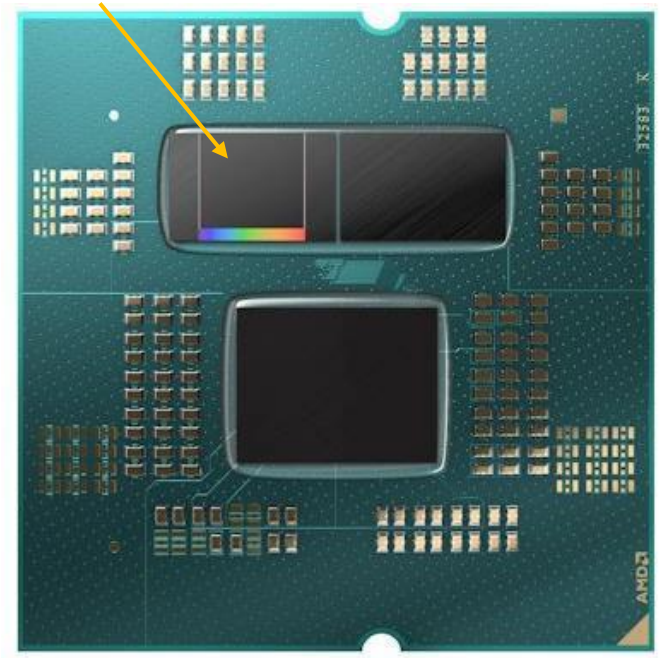


Ryzen CCD chip with TSVs attached to package substrate using standard flip-chip process

Ryzen™ 9 7900X3D

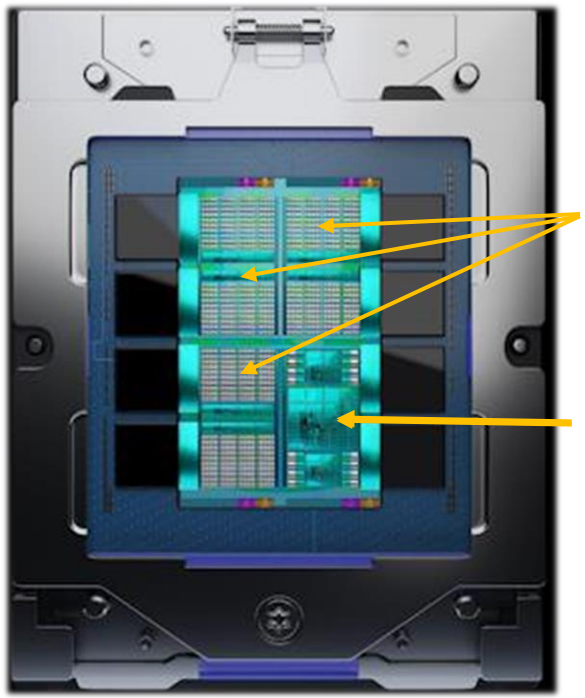
- **Gaming processor**
- Hybrid bonding of two Ryzen CCD chiplets + custom I/O chiplet

Hybrid bonded CCD chiplet



MI300

- **GPU + CPU for super computing**
- First **logic-on-logic** stacking with D2W hybrid bonding

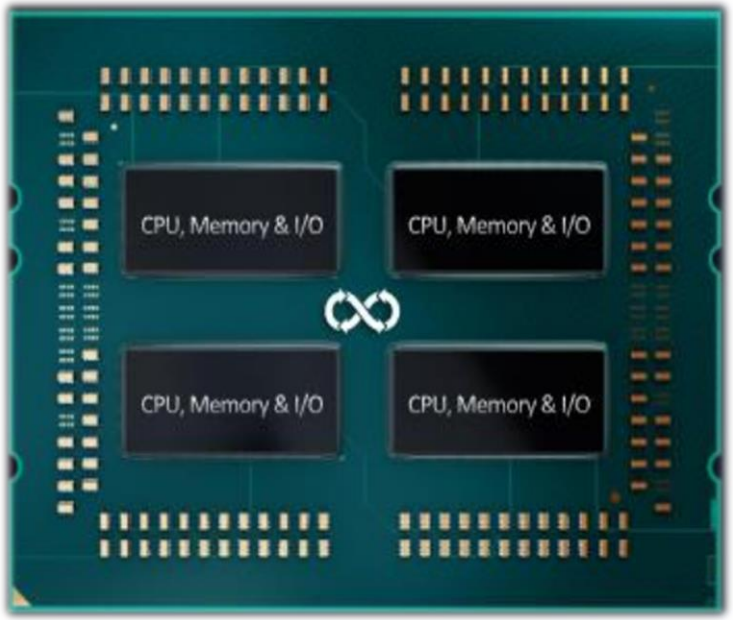


New Chiplet Architectures Increase Process Steps/Capital Intensity

2017 → **2019** → **2023**

1st Gen EPYC

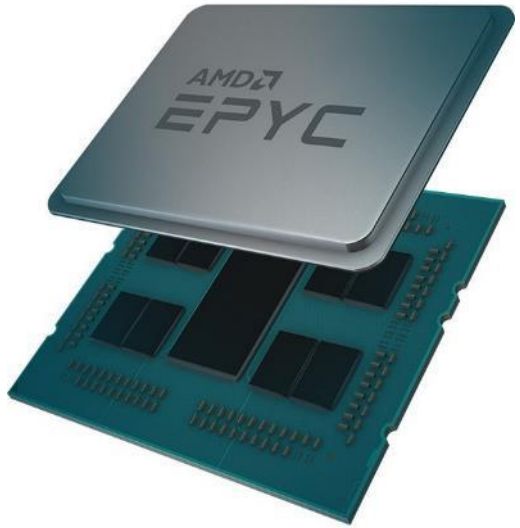
4 flip-chip placement steps



Source: AMD

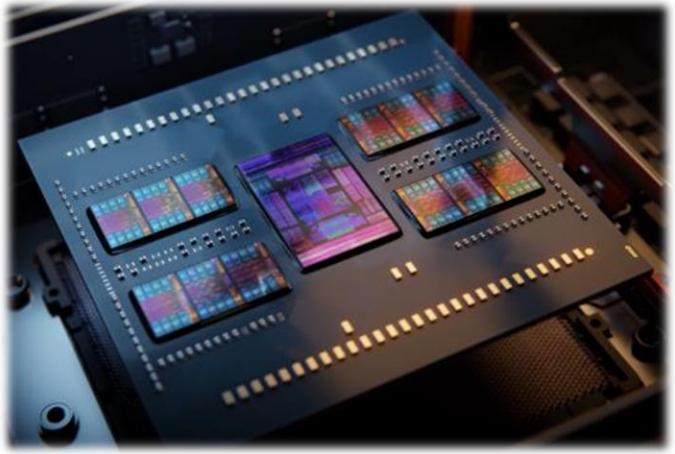
2nd Gen EPYC

9 flip-chip placement steps



4th Gen EPYC

> 50 die placement steps
including hybrid and flip-chip



Besi Process Solution:

8800 FC Quantum
ASP: $500k
UPH: ~9,000

→

8800 Ultra Accurate C2W Hybrid Bonder:
ASP: $1.5MM-$2.5MM
UPH: ~1,500 →~ 2,000

Industry Leaders Driving Adoption of Chiplet Standards

Standardization critical to incorporate heterogeneous chiplets from multiple producers in same package

- Universal Chiplet Interconnect Express (UCIe) emerging standard defining interconnect between chiplets in package
- Supported by leaders in HPC ecosystem
- Proprietary interfaces to still be used for core IP

Many benefits of standardization:

- Enables construction of SoCs exceeding maximum reticle size
- Reduces design time and time to market
- Incorporates high density and high-speed die-to-die interface
- Supports advanced package interconnects like Hybrid, TCB C2W and embedded fan-out bridge

UCIe Board Representatives

intel
AMD
Google Cloud
Alibaba Cloud
arm
Meta
NVIDIA
Qualcomm
Microsoft
tsmc
SAMSUNG
ASE GROUP

100+ members and growing

2.5D Interposer Market Expanding Rapidly From Small Base Currently

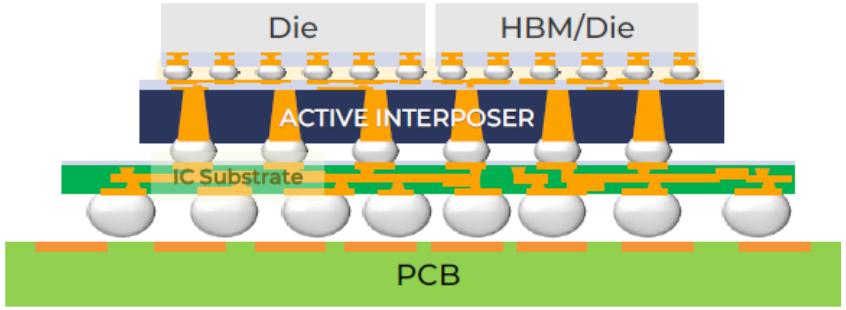
CoWoS = (Chip-on-Wafer-on-Substrate)

Highest growth rate for active Si interposer packages:
Intel Foveros and TSMC CoWoS-S

Multiple die attach steps:

- Chip-on-Wafer (CoW)
  - Requires flip-chip attach to the interposer
- On Substrate (oS)
  - Requires flip-chip of interposer to substrate

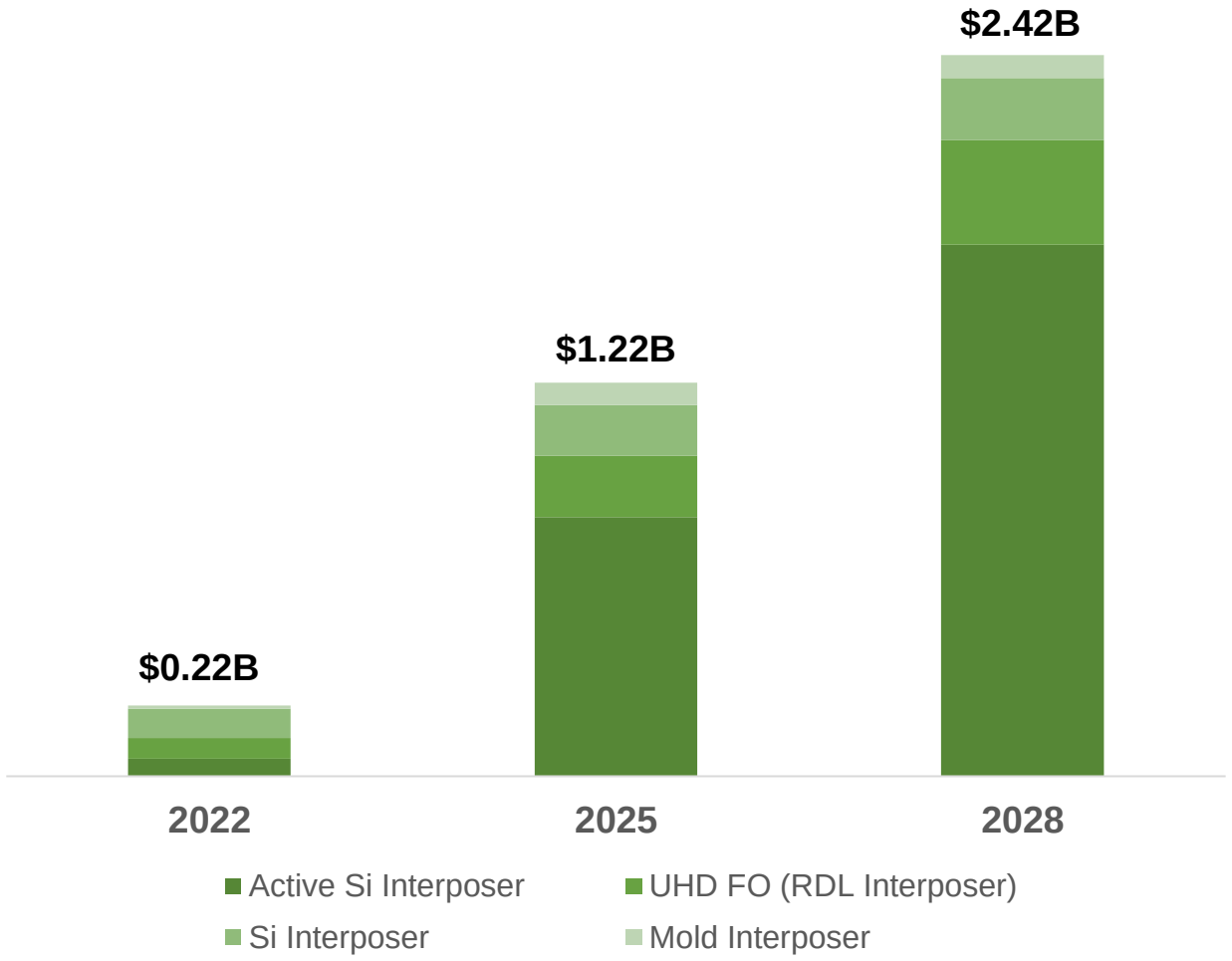
Besi equipment used for multiple process steps



Source: Yole

2.5D Interposer Package Revenue 2022-2028E

Source: Yole May 2023



What's Next in Mobile? New Features/Functionality in High End Smartphones and Wearables Drives Long-Term Growth

Mobile Data Traffic Growing Rapidly. Continued Deployment of 5G And Development of 5G Advanced Drives Need For Advanced Assembly Technologies

Advanced Camera Technology

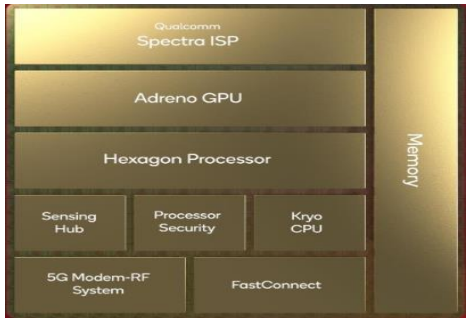
- Periscope and under display cameras
- New form factors

Source: CNET, Google

Source: GSMArena, Samsung

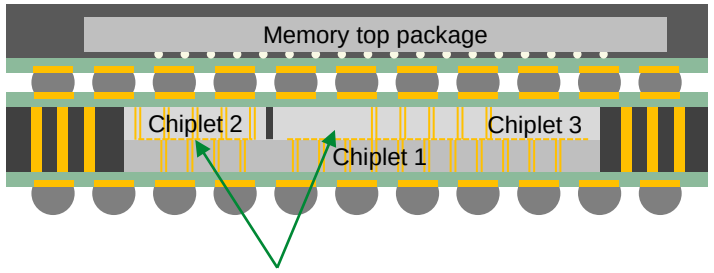
On Device AI

- Increased AI capabilities in AP chip
- AP die sizes increasing



Source: Qualcomm

- Potential chiplet architecture for application processor (AP) function



Hybrid bonded APU chiplet assembly

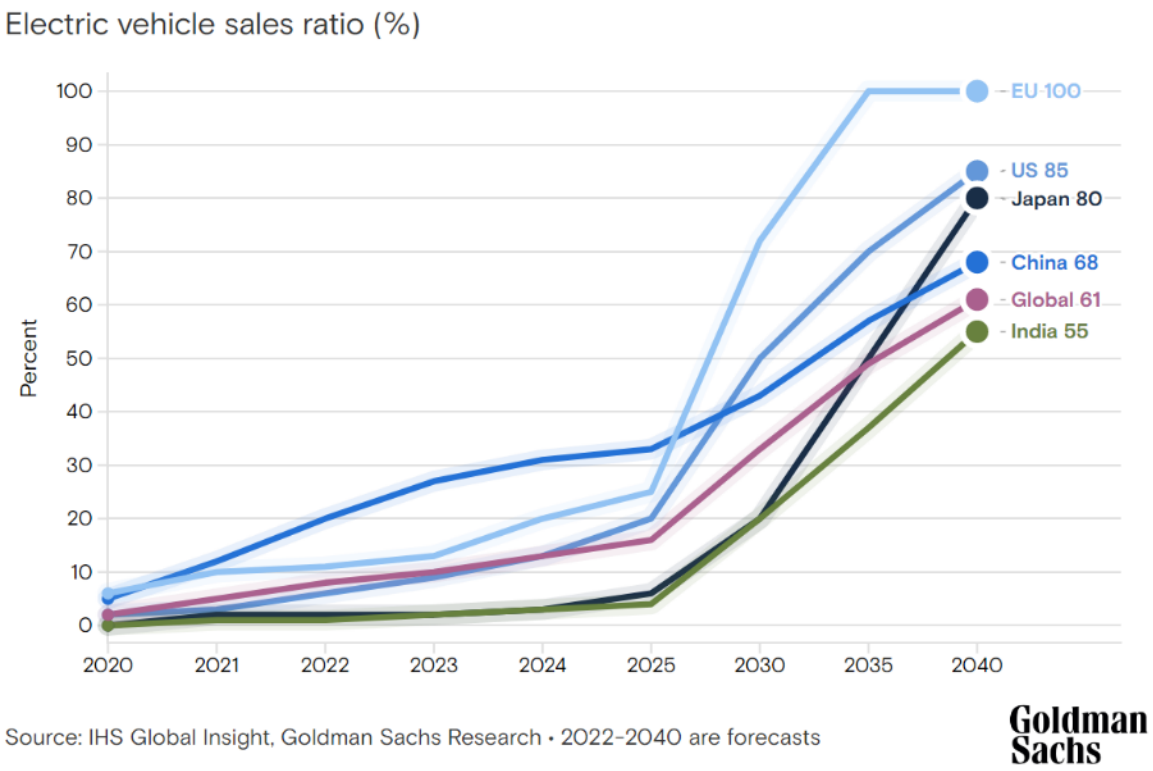
AR / VR Headsets

- New product introductions expected 2023 – 2024
- Requires extreme minaturization, 3DIC, TCB, advanced molding

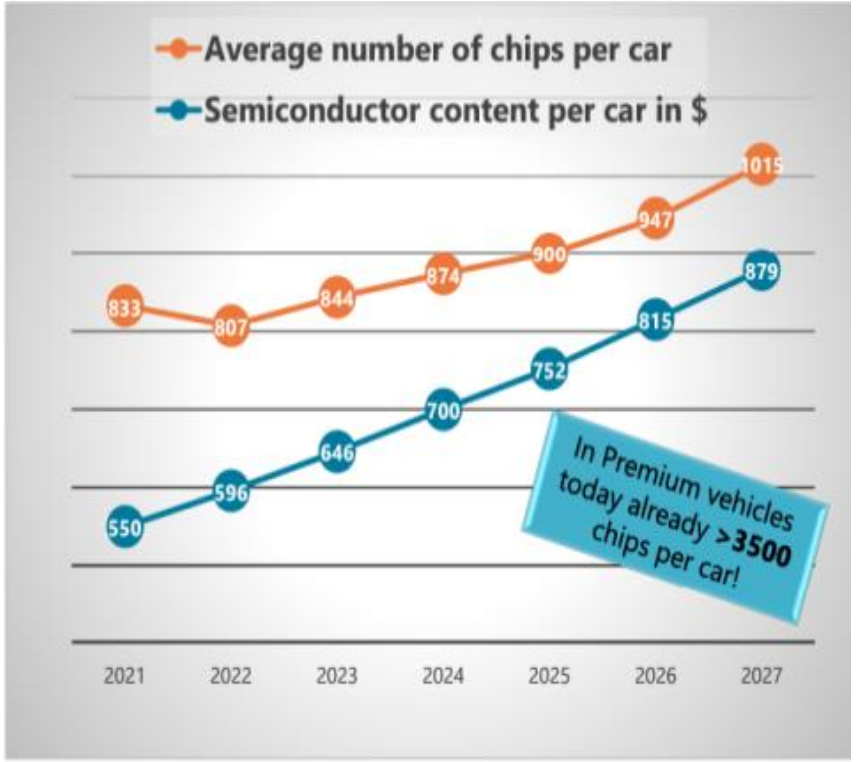
Source: Engaget

Automotive: Growth of EV and Autonomous Driving Will Increase Semiconductor Content and Cost per Car

Electric Vehicle Adoption Forecast to Accelerate



Semiconductor Content per Car Increasing



Source: Power Electronics News, January 2023

~12% CAGR in automotive semi sales (2021 – 2030)*

- 61% of global auto sales to be EVs by 2040
- Increased adoption of autonomous driving

*Source: Statistica, 2023

Positive growth trends anticipated to continue

- More sensors: cameras, radar, ultrasonic, LIDAR
- Increased use of AI, V2E connectivity

Rapid Growth in SiC and GaN Power Devices for Automotive Will Aid Each of Besi's Product Groups

SiC – 30% CAGR 2022 – 2028

High-speed operation and lower power loss

- xEV
- High power EV Charging
- Energy Storage
- Solar

GaN – 53% CAGR 2022 – 2028

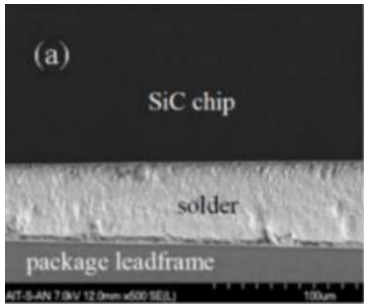
High efficiency, fast power switching

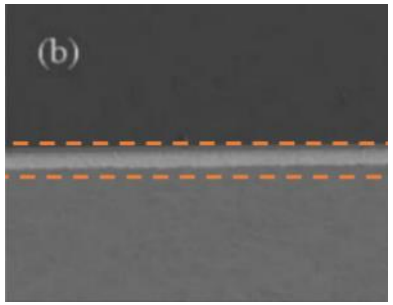
- On-board Charger
- 5G Base Station
- Portable Charger
- Server

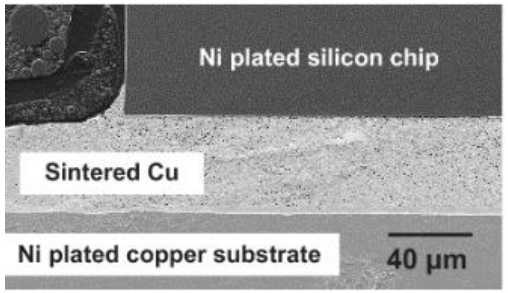
Source: Infineon May 2023

Requiring New Assembly Solutions

High Performance Power Die Attach







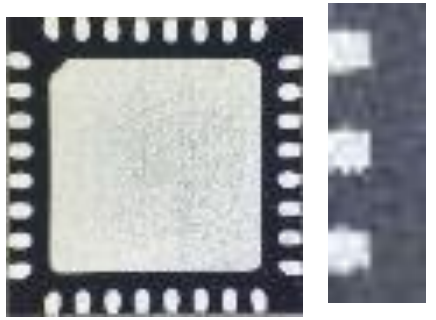
Source: Infineon

Soft Solder | Diffusion Bonding | Sinter Bonding

Module Packaging

Leadframe Plating

Mold Adhesion Process



Market Trends Favorably Position Besi for Long-Term Growth

Slowing of Moore's Law drives chiplet architectures and hybrid bonding adoption

- Increasing cost per transistor in advanced nodes drives new chiplet solutions
- Hybrid bonding adds a new dimension to enable system scaling besides node shrinkage
- Chiplets = more die placement steps using higher precision equipment = higher capital intensity
- Besi major beneficiary

Next gen HPC will drive growth in computing end user markets

- Data volumes growing exponentially
- Generative AI, Big data, HBM, edge computing, photonics require new substrate and wafer level assembly solutions

New technologies on horizon will drive growth in Besi's mobile market

- 3D IC integration, advanced camera systems and deployment of mmWave 5G
- New wearable devices with challenging form factors & advanced cameras
- Potential adoption of hybrid bonding in HBM Memory devices, mobile processors

Transition to EVs with autonomous driving will drive high end automotive demand

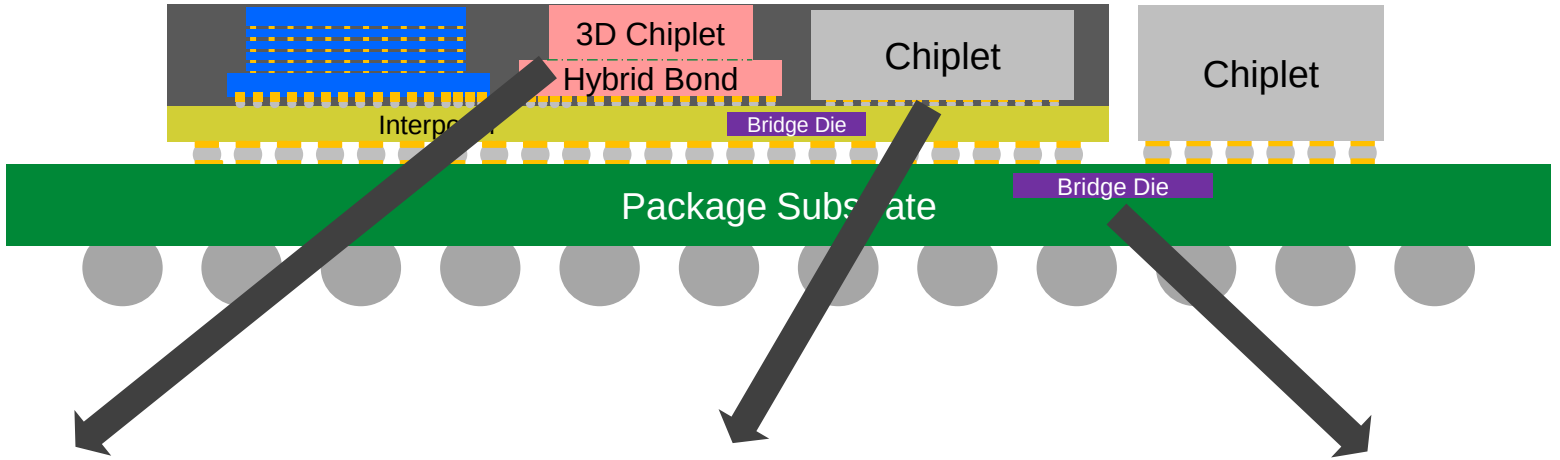
- New SiC and GaN power devices requiring new die attach, packaging and plating processes
- Increased sensing and on-board computing content for safety and automation

III. Wafer Level Assembly

Peter Wiedner

Senior VP Sub-Micron Die Attach

Three Principal Wafer Level Die Bonding Platforms



Hybrid Bonding

- 8800 CHAMEO ultra plus
- 8800 CHAMEO ultra plus AC

Q1'24

Thermo Compression

- 8800 TC *advanced*
- 9800 TC *NEXT*

New

Embedded Bridge Attach

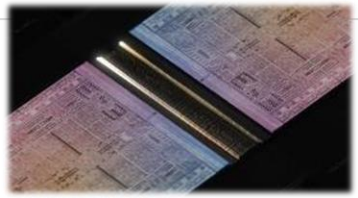
- 8800 CHAMEO *ultra*

Chiplet Designs Require Ever Smaller Interconnect Pitch and Higher Contact Density

Transition to Wafer Level Assembly with Sub-Micron Accuracy

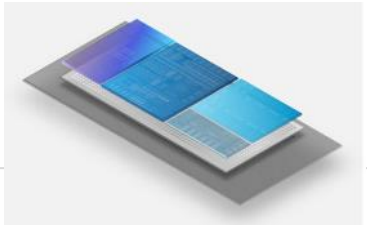
MI 300

M1 Ultra
Fan-out Bridge



Source: Apple

Meteor Lake
TCB Chip-to-Wafer

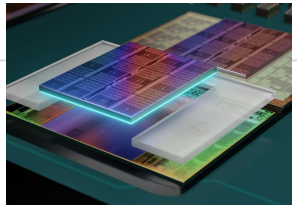


Source: Intel

Sapphire Rapids
EMIB - TCB

Source: Intel

3D VCache
with Hybrid Bonding



Source: AMD

Contacts per Square mm

1,000,000
100,000
10,000
1,000
100
10

Hybrid Bonding
TCB C2W
Fluxless
TCB C2S
Laser Assisted (LAB)
Flip-Chip

0 10 20 30 40 50 60 70 80

Interconnect Pitch (µm)

8800 Chameo Ultra Plus: Reflects Industry Shift To Smaller, Integrated, Heterogeneous Chip Designs

Leading Hybrid Die Bonding System on Market

- Direct Cu-Cu Interconnect
- Design Flexibility
- Lower Cost of Ownership
- Ultra-High Bandwidth & Speed

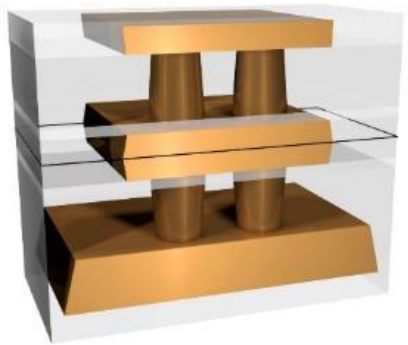
Target Markets & Customers

- **Computing**: Chiplet integration for HPC Heterogeneous integration
- **Memory**: High density 3D NAND
- **Consumer**: Application Processors & CMOS

Key competitive advantages

- Patented Van Gogh bond head and vision system
- **< 200 nanometer accuracy**
- **Speed range: 1500 - 2000 UPH**
- **High production yield achieved**
- Front-end clean room standard
- Full front-end automation including tool changes

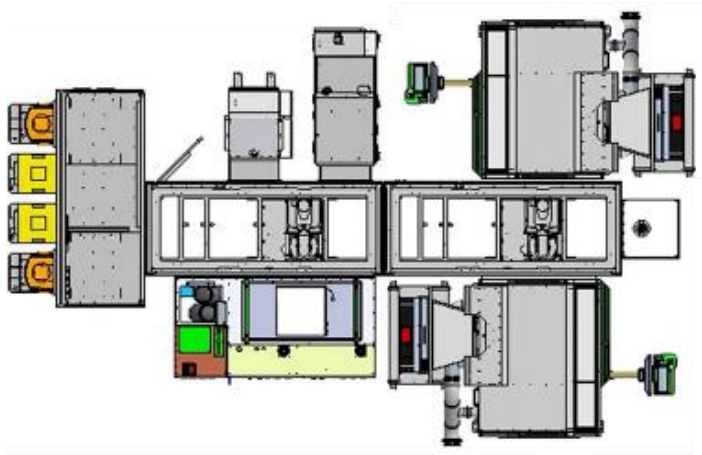
Logic: 100 nm accuracy



Memory: Die Stacking

AMAT Joint Development

- Relationship since 2019
- Anticipate expanding cooperation
- CoE fully operational since 2022
- Engagement with all leading players



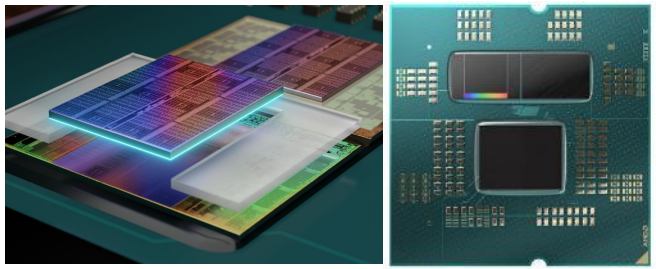
Cluster Tool:
Fully integrated Hybrid Bonding Solution

COE Singapore:
Shared facility for Development and Customer Demos

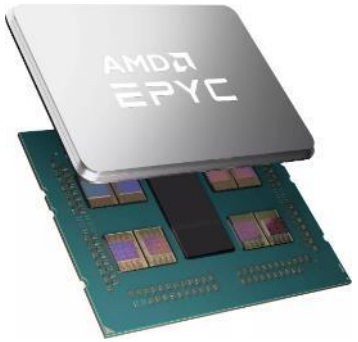
Center of Excellence provides a fully integrated hybrid bonding production environment

Hybrid Technology/Market Roadmap

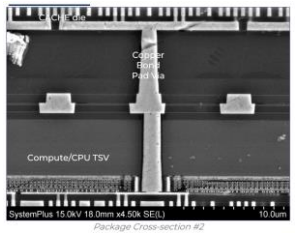
First HB Product Launched
AMD Ryzen 9 7900X3D



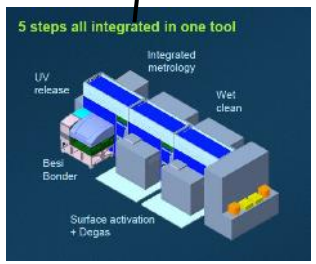
Additional Product Launches
AMD EPYC, Milan X



Q3/22 | Q4/22 | Q1/23 | Q2/23



200 nm Bonders installed for HVM

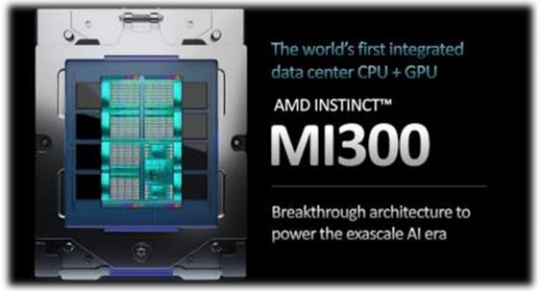


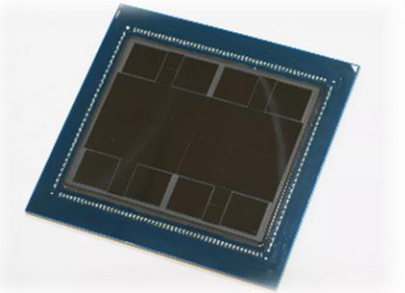
First integrated production line shipped

First 100nm R&D Bonder shipped for product qualification

Future Hybrid Technology/Logic Market Roadmap

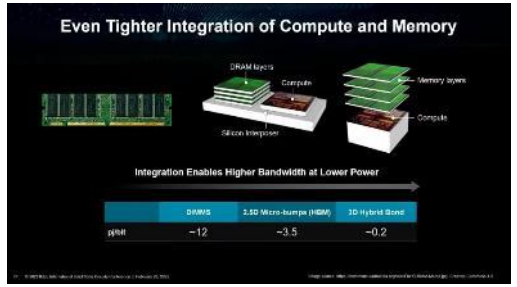
AMD MI 300 super computer to launch Summer 23 with >13 hybrid bonded chiplets



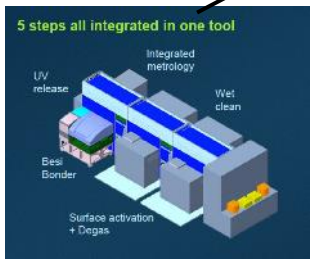


Second major logic customer confirmed HVM ramp

Next gen products incorporate even greater Hybrid integration

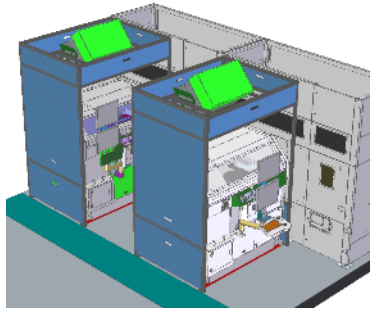


Q3/23 | Q4/23 | Q1/24 | Q2/24



Additional cluster shipments incorporating multiple Bonders

100 nm production HBs to be shipped to beta customer



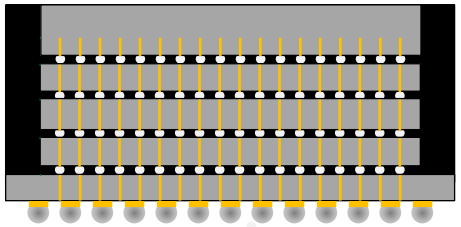
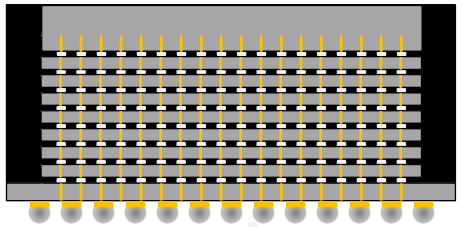
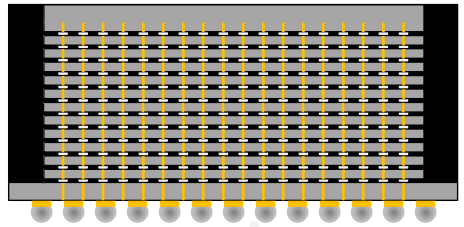
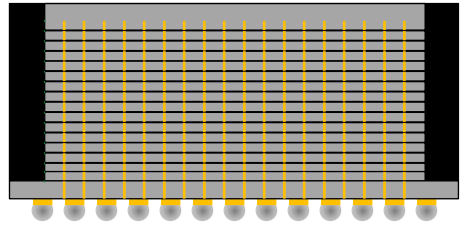
8800 CHAMEO ultra plus AC (100 nm) ready for HVM

HBM Stacking Will Drive Even Further Capital Intensity

Image source: Techsearch

Hybrid Bonding can be used to stack 16 or more die, starting with HBM4

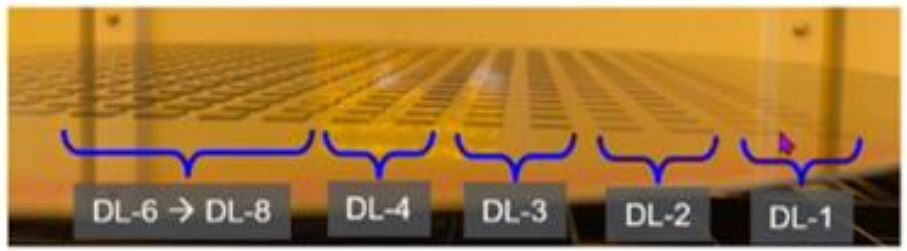
- HBM mounted beside high-performance CPU or GPU on interposer
- Height of HBM stack no greater than XPU chip thickness
- **36% of HBM will use hybrid bonding by 2028 according to Yole**

2014	2018	2022	2025-26
HBM1	HBM2	HBM3	HBM4
			
4 Memory Chips	4 - 8 Memory Chips	8 -12 Memory Chips	12 - 16 Memory Chips
			Hybrid Bonding

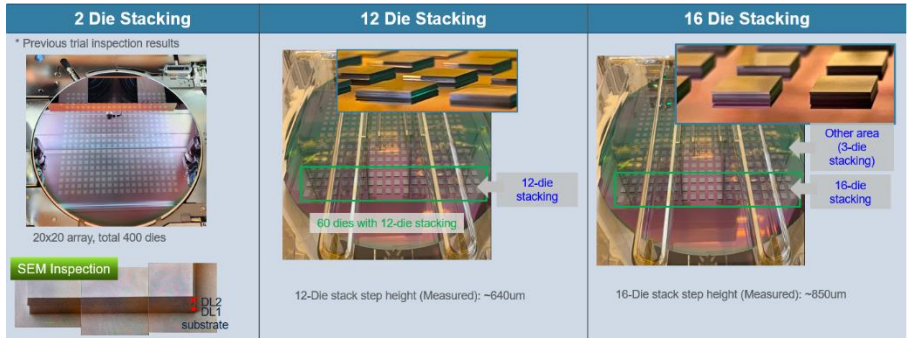
Solder bumps used for stacking

Future Hybrid Technology/Memory Market Roadmap

COE Singapore: first samples built in 2023

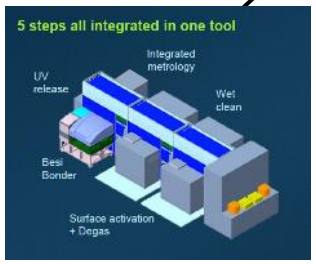


Further sampling and development by leading memory producers

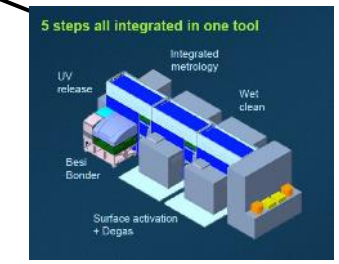


22 | Q2/23 | Q3/23 | Q4/23 | Q1/24

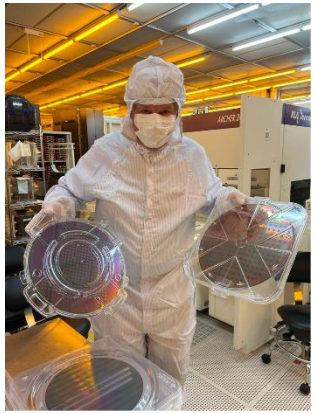
Demo Bonder shipped to first memory customer



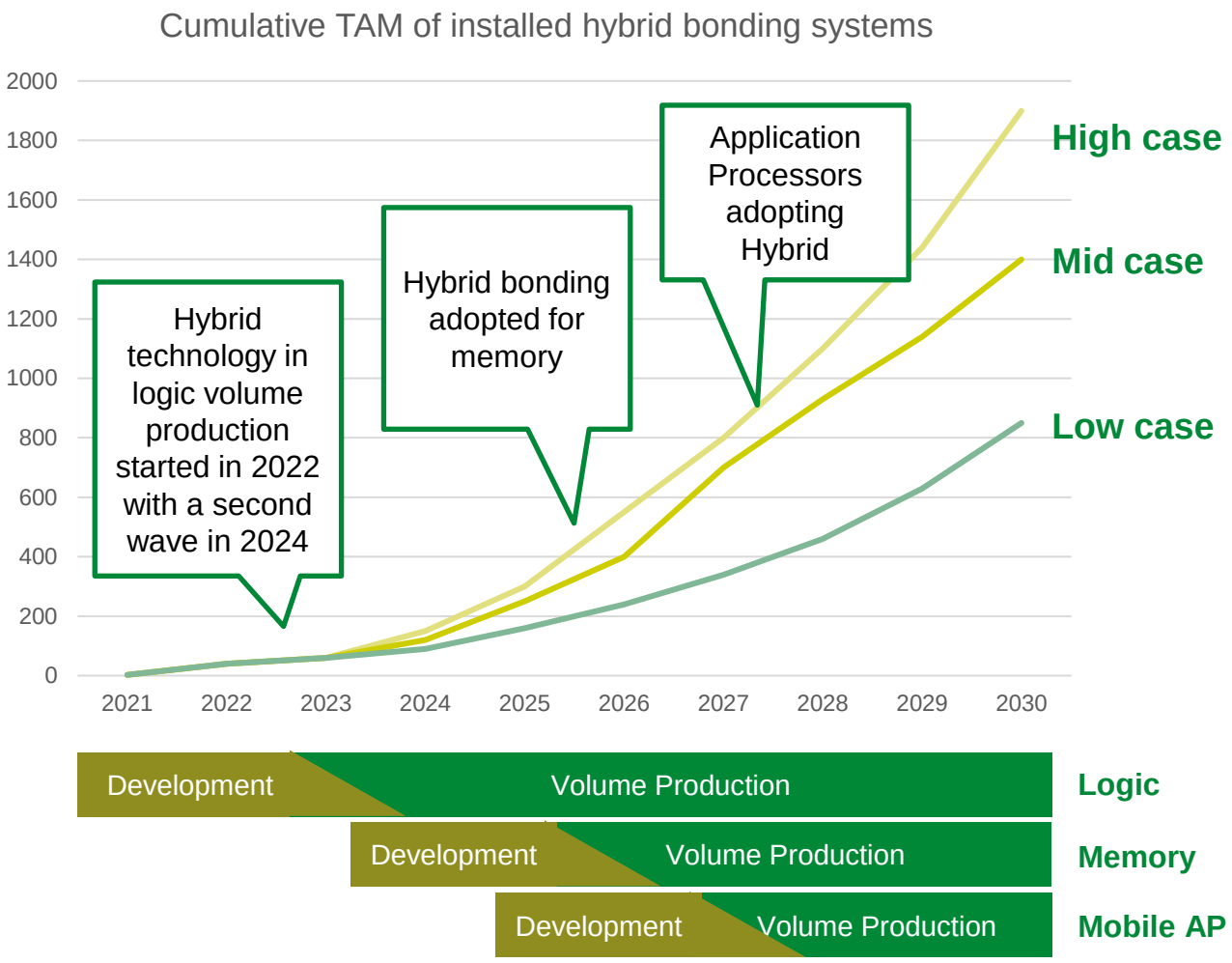
1st Memory cluster tool shipment



2nd Memory cluster tool shipment



Hybrid Bonding Market Potential



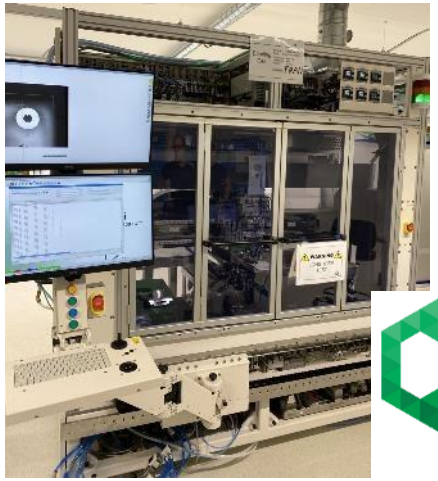
Source: Besi estimates, June 2023.
Cases based on potential adoption scenarios.

Estimated 800 – 1,900 systems cumulative by 2030

- Logic device production and adoption continues
- Low case represents adoption in logic only
- Technology adoption coming in waves
- Major memory companies engaged for HBM programs
- Increased interest for HB usage in consumer applications
- **Changes to market forecast vs. CMD ‘22**
  - **Upside and low case unit potential expanded**
  - **Tracking to mid case currently**
  - **Higher ASPs anticipated due to higher accuracy requirements post 2024**
- Expected rollout sequence:
  1. Logic
  2. Memory
  3. Mobile
  4. Other Applications

Next Generation TCB C2W System Important in Wafer Level Roadmaps
First System Sold in Q1-23

9800 TC^{Next}



Target Markets & Customers

- **Computing**: HPC, Heterogeneous Integration
  Si interposer attach
- **Memory**: HBM stacking

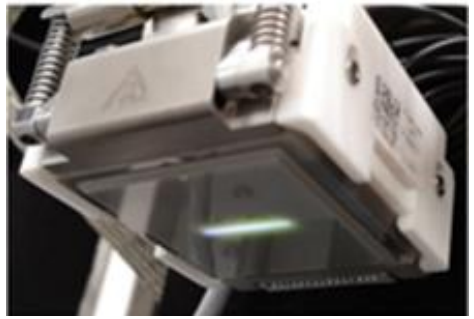
intel IBM tsmc SAMSUNG Micron

- Market for logic primarily 1 customer currently. New customers evaluating
- TCB for memory will probably be used to stack up to 12 dies

Key competitive advantages

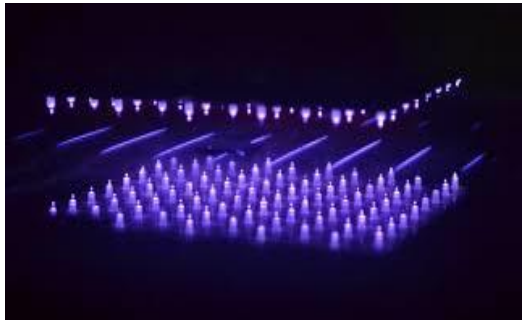
- Both chip-to-substrate and chip-to-wafer capabilities
- Flexible material handling
- Bond collapse detection
- Ultra-low gas usgae
- **Up to 70mmx70mm die size**
- **Submicron accuracy**
- **Prepared for fluxless**

High accuracy for big die sizes



Sub-micron accuracy
for chiplets

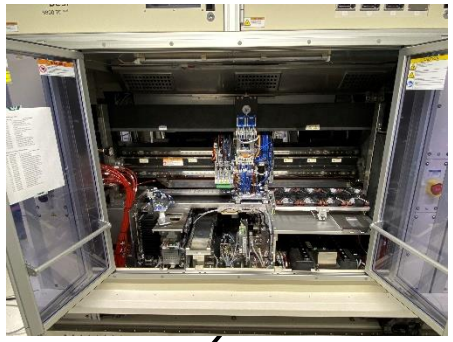
Fluxless process



Smaller pitches
require fluxless process

Besi's TCB C2W Development Roadmap

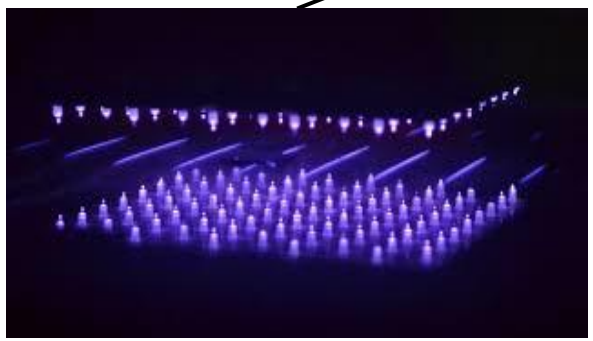
1st system sold to lead customer



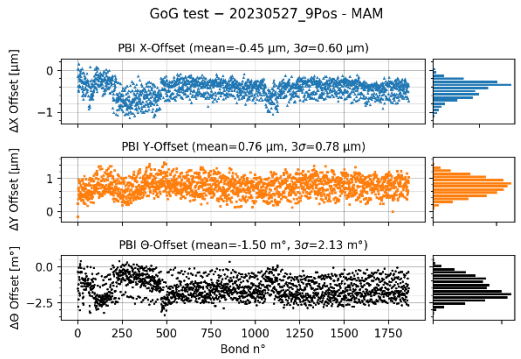
Production system to be shipped

1st Memory Demo system to be shipped

Q2/23 | Q3/23 | Q4/23 | Q1/24



Fluxless Process Development



Next accuracy step: 800 nm

IV. MAINSTREAM DIE ATTACH
Christoph Scheiring
Senior VP Die Attach

Besi Die Attach Summary

Revenue	~70% of BESI
Market Share	~40% in Die Attach ~75% in Advanced Die Attach
Market	Die Attach 12.2% CAGR (2020-2025)*
Drivers	Mobile, Auto, Computer

Source: TechInsights May 2023

Industry Leading Die Attach Equipment Portfolio

Multi-Module Attach

- 2200 evo
- 2200 evo *plus*
- 2200 evo hS
- 2200 evo *advanced*
- 2200 evo hf

Die Bonding

- 2100 hS
- 2100 hS i
- 2100 sD *advanced i*
- 2100 hS ix

Multi-module

Mainstream Epoxy

FlipChip

SoftSolder

Flip-Chip

- 8800 FC Quantum *adv*
- 8800 FC Quantum *hs*
- 8800 CHAMEO *advanced*
- 8800 CHAMEO *Ultra*
- 2100 FC hS

Soft Solder

- 2009 SSI
- 2100 SSI

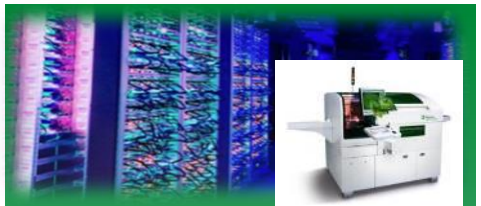
Die Attach End-User Market Positioning

REVENUE

Multi Module Attach
- Camera&Sensing

Die Bonding
- 5G
- IoT / Wearable

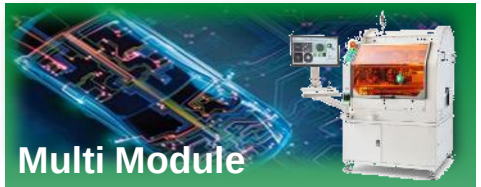
Mobile



FlipChip
- CPU/GPU
- HPC

Multi Module Attach
- HDD/Server
- HPC, CoWoS

Computing



Multi Module Attach
- Power modules

SoftSolder
- Discretes
- Modules

Automotive

2200 Multi-Module Attach: Industry Leading Multi-Die Platform

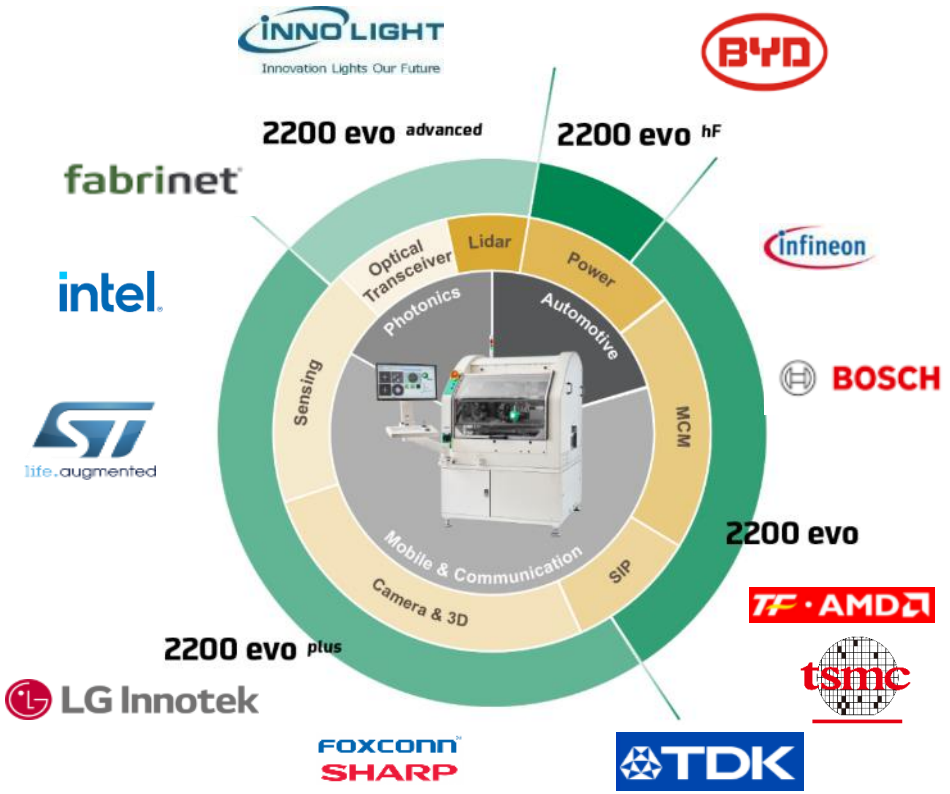
Continuously Upgraded for New Applications

> 7,000 Units Shipped

Key competitive advantages

- Multi-die, multi-wafer
- High accuracy and high speed
- Highly configurable
- Broad range of applications
- Rapid R&D to production

Target Markets & Customers



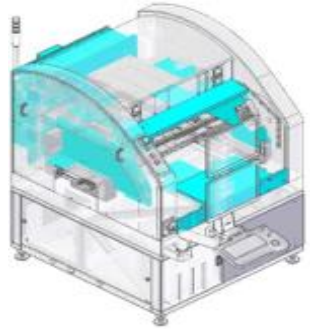
Highlights 2023

Advance Camera Assembly

POR for NextGen Periscope camera

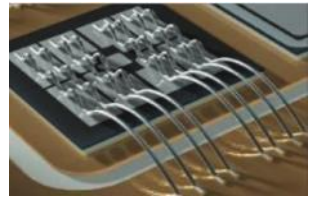
Increased Cleanliness

Significant yield improvements for advanced camera modules



Increased Bondforce

New High Force model gaining traction in Power Sintering



Source: Semikron

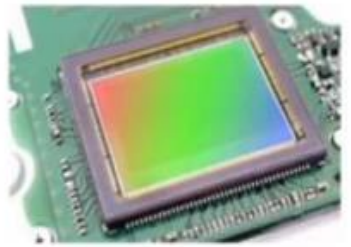
2100 Epoxy Die Attach: Industry Leading Platform
Highest Speed and Accuracy for Single Die Placement

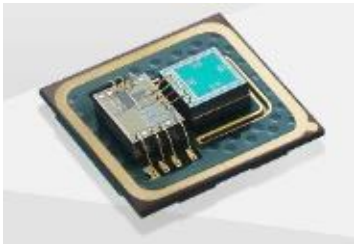
> 4,000 Units Shipped

Target Markets & Customers

- **Mobile, 5G:** PA, RF front end modules, Sensors, PMIC, analog
- **Automotive**: MEMS and Sensors, Auto CIS
- **Storage**: NAND
- **Industrial**: Analog, power, MCU

ChipMOS, TF, ASE, HUA TIAN, UTAC, NXP freescale, Infineon, JCET STATSChipPAC, GREATEK ELECTRONICS INC., Carsem, Amkor Technology, qorvo





Key competitive advantages

- Industry leading accuracy and speed
- Precise bond line thickness control
- Confocal scanning for real time material height and epoxy volume compensation
- Ultra-thin die and cleanliness
- Automation: AGV loading

Highlights 2023

Automotive MEMS

- Good traction MEMS/Auto with dispensing volume control features
- EU expansion expected
  - Due to geopolitical tensions
  - Driven by EU tier1 suppliers

6 Side Die Inspection

- Major installation for NAND chipping inspection in TW
- AI improving vision algorithms

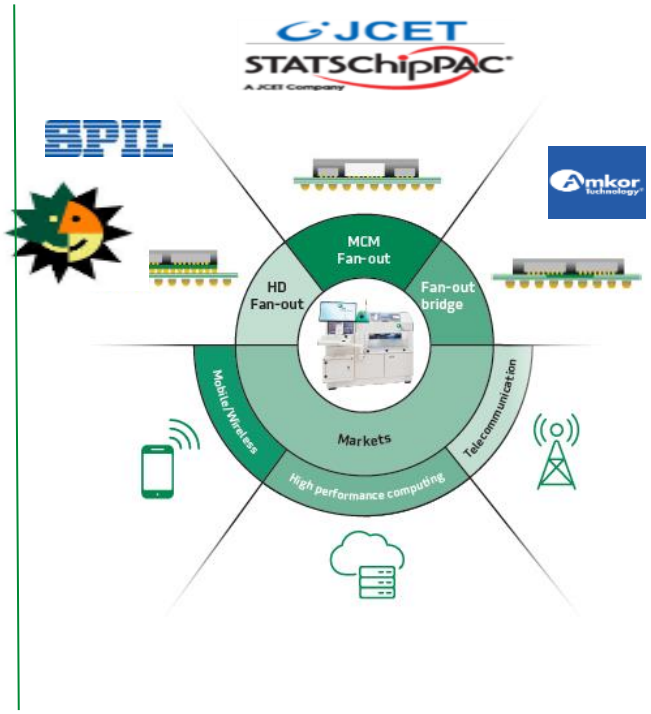
Auto CIS

- Qualified 2100 platform for Auto CIS product (EU Auto OEM)

Industry Leading Flip-Chip Product Portfolio

Advanced Flip-Chip, Fan-out and Bridge Attach
8800 CHAMEO

- Accuracy: < 3 (1) µm
- Throughput: 10,000 UPH
- Die size: 40mm, 300mm substrate
- EFEM Loader, Factory Automation
- ISO 5 cleanliness



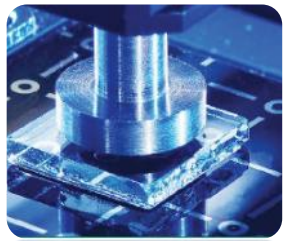
Mass Reflow Flip-chip
8800 QUANTUM & 2100 FC hs

BGA, CSP, 5G SiP, Memory

FCoLf / QFN / Led / SiP

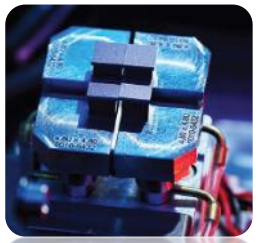
Highlights 2023

Advanced Packaging
- Best in class offering for chiplets +HD Fan-Out (1um local accuracy)



Automation
- Fully qualified factory integration solution

High Speed FC
- New customer/market penetration
- Superior multi-eject & multi nozzle concept

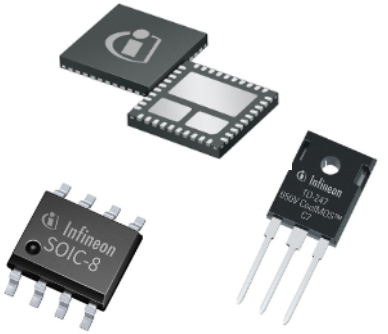


2100 Soft Solder System: Quantum Step Forward for Automotive and Industrial Applications

Next Generation Soft Solder

Target Markets & Customers

- **Automotive**: High Rel Power packages, SiC, Diffusion Bonding
- **Industrial**: All power devices, IGBT, IPM, Clip Bonding



Source: Infineon Technologies

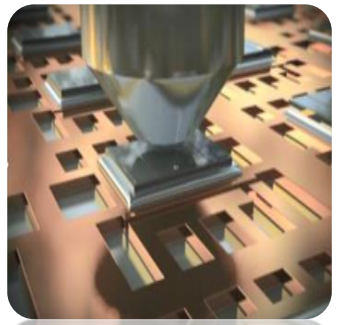
Key competitive advantages

- **Leading soft solder process**
  - Low oxygen level
  - Lowest gas consumption
  - Fully automotive qualified
- **XLF leadframe handling**
- **POR for key automotive IDM**

Highlights 2023

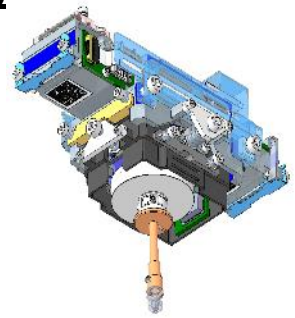
Product Proliferation

- Platform succesfully qualified at major Auto IDM's,
- Multiple systems in HVM
- Next customer qualification
- expected in H2'23

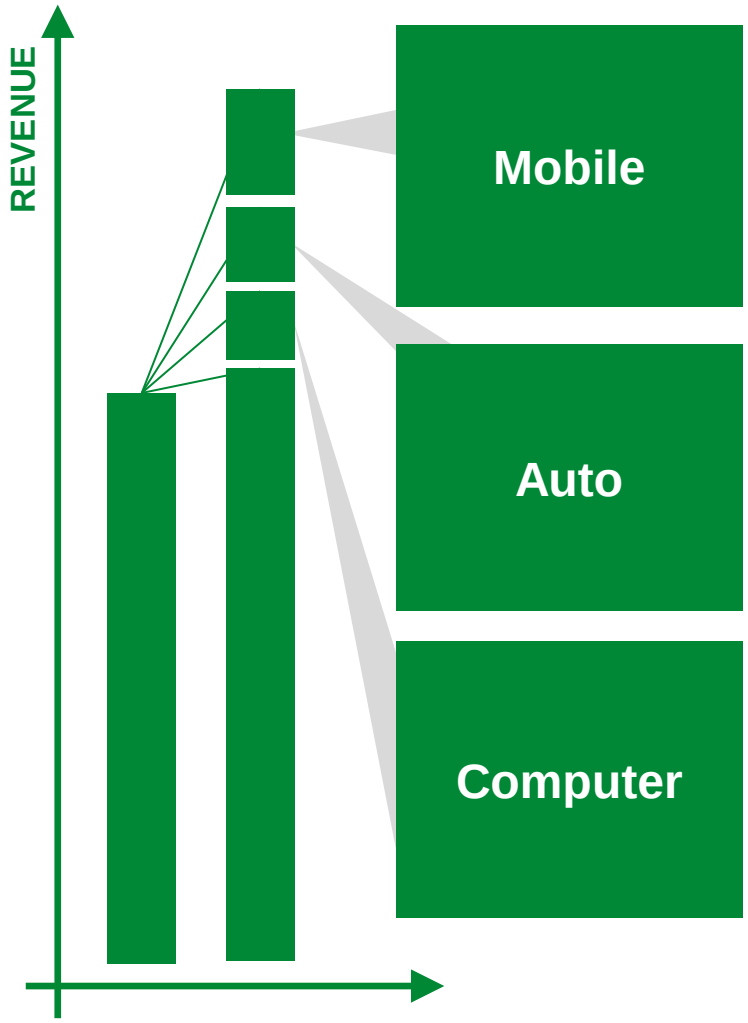


Process Superiority

- Diffusion soldering in qualification at major customers
- Key differentiators:
  - Cleanliness,
  - Bondforce
  - Oxygen control



Key Die Attach Growth Drivers and Development Projects



DRIVER

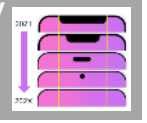
- Advanced Camera Functionality
- Under display biometric identification
- New Devices AR / VR

- EV adoption
- ADAS

- 2.5/3D & chiplet architectures
- Photonics

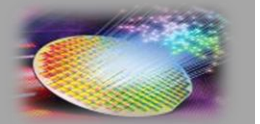
KEY TECHNOLOGY

- Periscope camera modules
- Integrated sensing/camera/display



- SiC/GaN
- Sintering
- Diffusion Soldering

- HD Fan-Out / Bridge Attach
- Optical Transceivers



V. PACKAGING
Jeroen Kleijburg
Senior VP Packaging

Best in Class Packaging Portfolio
Focused on Leading Edge Applications and Customers

5G and Wearables

IoT/Computing

Automotive

Storage and Network

Substrate Molding

AMS-LM
- Two sided substrate molding
- Exposed die;
- Wearables (SIP)

Substrate Singulation

FSL
- Substrate strip singulation
- Sorting
- Stepcut

Wafer & Panel Molding

FML
- Wafer molding
- Panel molding

Leadframe Molding

AMS-X
- HD Leadframe
- Power Devices

Trim and Form

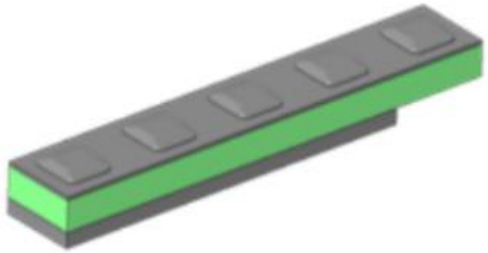
FCL-X/P
- Leadframe trim & form
- Sorting

Molding: AMS LM Substrate Molding: Leading Exposed Die System for 5G and Complex 3D Molding Applications

350+ Systems Shipped

Target Markets & Customers

- **5G** : Advanced RF front-end modules
- **Wearables** : SiPs with intricate 3D designs
- **Memory** : Stacked Die and FC DRAM 5



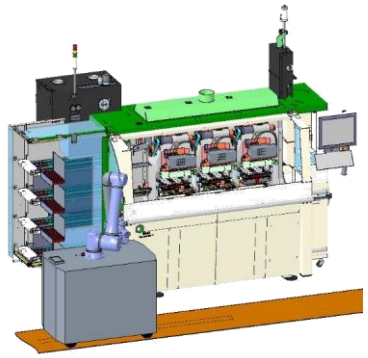
Key competitive advantages

- Best in class COO
- Lowest power usage and weight
- Standard for thin die molding
- Exposed die molding (90% share)
- Dynamic clamp force control
- Board thickness compensation
- Double sided molding (5G FEM)

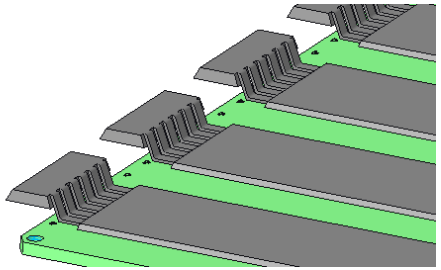
New Developments 2023

AMS-LM MK3 System

AGV Handling



Void Reduction

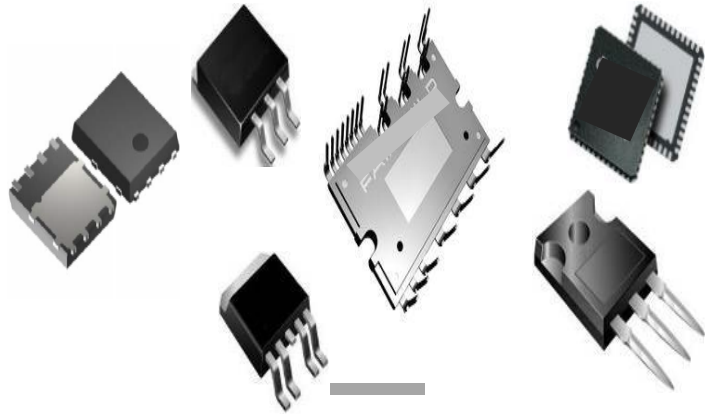


Molding: AMS-X Leadframe Molding: Power and SIP Packages for Automotive and Industrial Market

First systems in production

Target Markets

- **Automotive**: High rel power packages, SiC
- **Industrial**: All power devices, IGBT, IPM

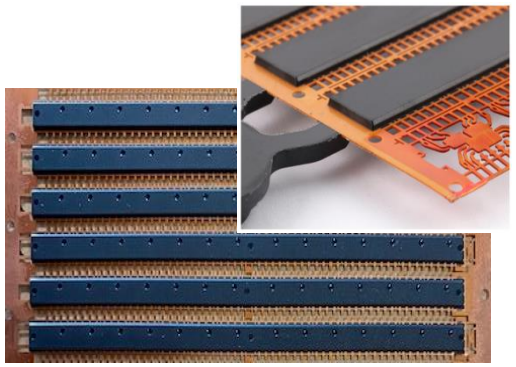


Key competitive advantages

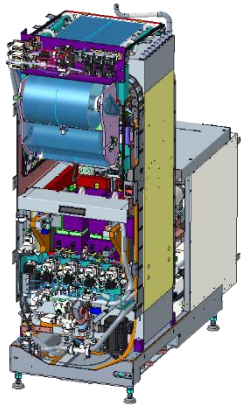
- 20% less energy consumption
- 12% less compound loss
- Modular concept (modules used from T&F and singulation)
- High cavity vacuum of 50 mbar
- 4 individual clampforces
- No vibration due to low weight
- Leadframe size up 125 mm

New Developments 2023

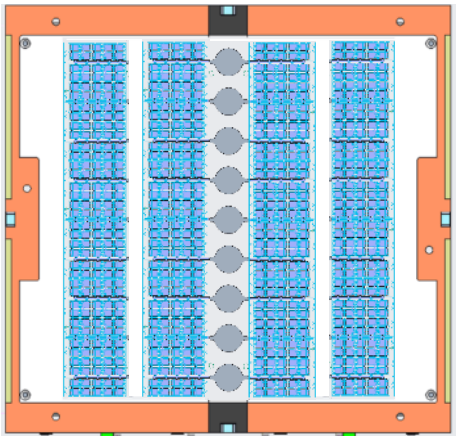
Bar Molding



Top Foil



Reduction of COO

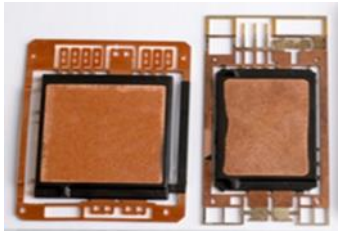


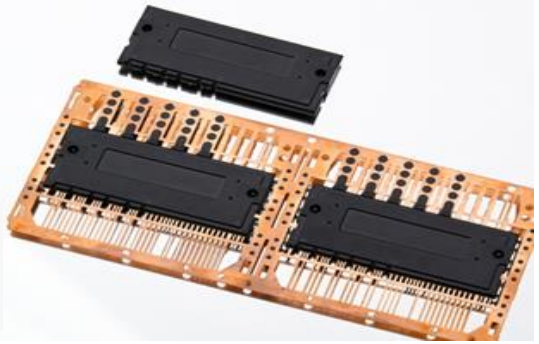
Trim & Form: Fcl-x for Power and SIP Packages for Automotive and Server Markets

1500+ Systems Shipped

Target Markets

- **Server** : System in packages
- **Automotive** : IGBT, SO and TSOP packages





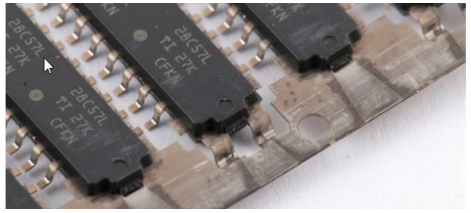
Key competitive advantages

- Zero defect
- Advanced vision (up to 30 inspections)
- Individual package marking
- High speed reject punching
- Highest UPH (up to 220 str/min)
- Flexibility by common modules

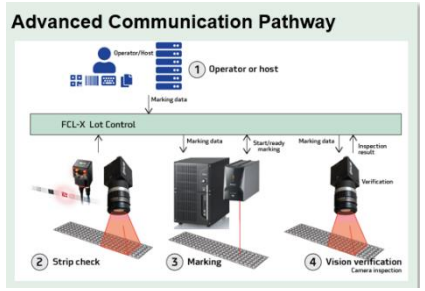
New Developments 2023

Focus on power packages

Pitch Correction



Integration



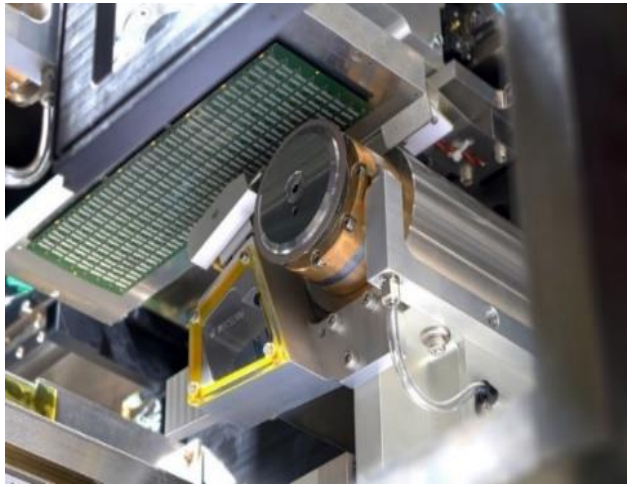
AGV Handling

Singulation: FSL Stepcut Leadframe: Power and SIP Packages for Automotive and Server End Users. Gaining Market Traction

Singulation

Target Markets

- **Server** : System in packages
- **Automotive** : SOIC and TSOP packages
- **Memory** : Stacked Die and FC DRAM 5
- **5G** : Advanced RF front-end modules



Key competitive advantages

- Step-Cut: ±20µm with Cpk > 1.33
- Size & Offset: ±25µm with Cpk > 1.67
- Warpage Handling (short): < 12mm
- Warpage Handling (long) < 18 mm
- Conversion time less then 5 minutes
- Stack magazine offloading with step cut
- 35% less water consumption

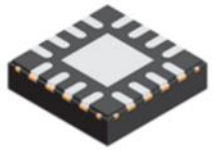
New Developments 2023

High speed sorting

> 45K UPH with tray offload

Step cut

Increases reliability



Tie bar-less sawing

Wafer Level Molding For Chiplet Applications

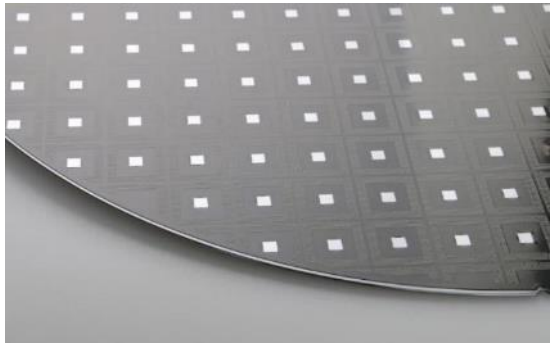
Emerging Process Technology

FML

Target Markets

- **Computing**: Chiplet integration for HPC
  Heterogeneous integration
- **Mobile**: 3D Wafer level fan-out

Wafer level mold with exposed die



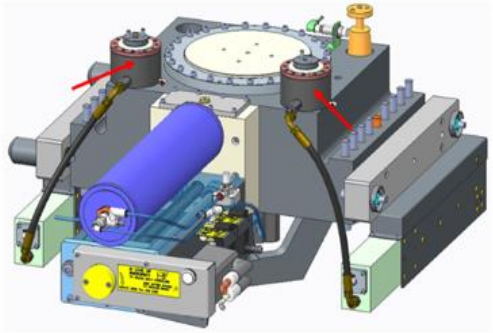
Key competitive advantages

- Exposed die wafer molding
- Wafer level molded underfill
- Narrow gap filling < 50 µm
- Dynamic clamp force control
- Mold planarity below 5 µm
- High precision wafer placement
- 150 ton capability

New Developments 2023

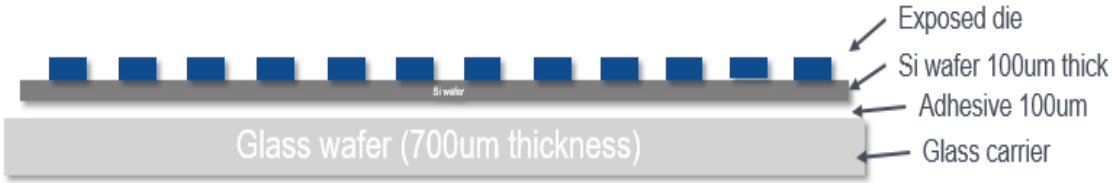
Auto leveling

Precise thickness across wafer

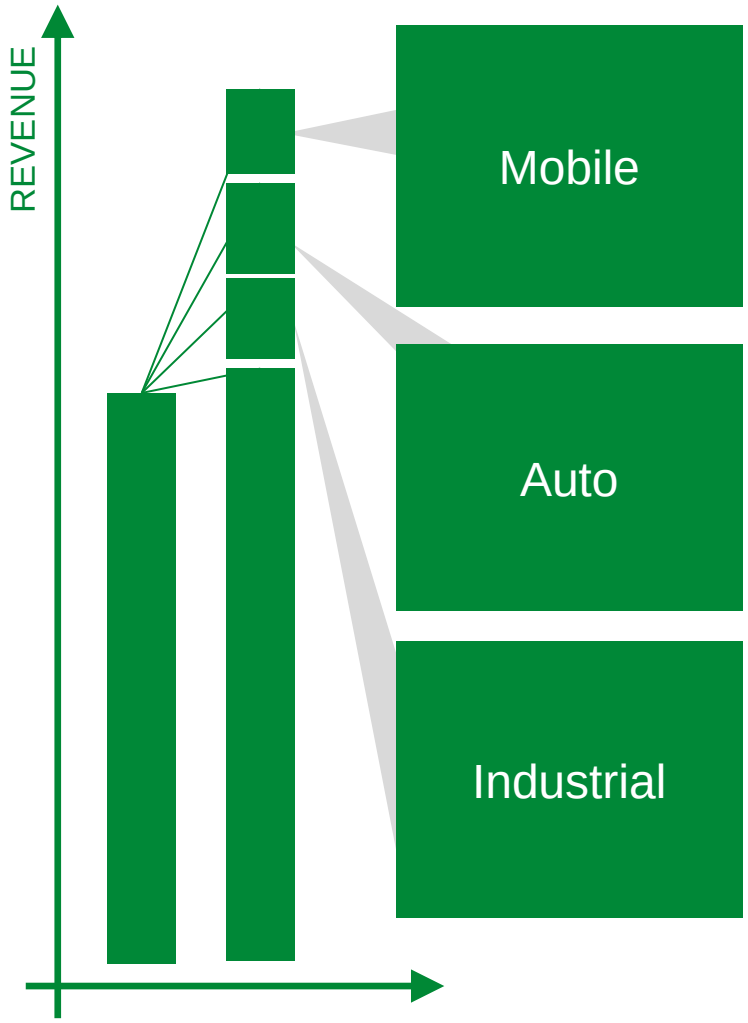


TSV Wafer molding

Exposed die molding to encapsulate hybrid bonded die



Packaging Growth Drivers and Key Development Projects



DRIVER

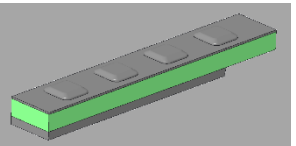
- 5G mm Wave
- 3D Image Sensing

- Power switching
- Battery charging
- Battery management
- Safety management

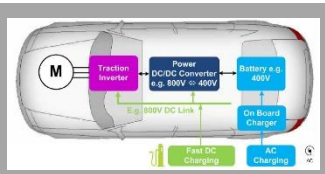
- Energy transition from-fossil fuels
- Factory Automation 4.0
- On-shoring of production

KEY TECHNOLOGY

- SiP packages
- Battery management unit
- Wearables



- SiC/GaN
- High density frames
- Silicon Gel To Expoxy



- Silicon Gel to Epoxy
- Single unit handling
- Double side cooling

VI. PLATING
Bart Berenbak
VP Plating

Besi Plating: Dominant Market Share In Leadframe Plating For Automotive/Industrial Power Markets

Leading plating equipment for a range of wet chemical surface treatments

- Technology leadership since 1978
- Key supplier to leading IDM's and OSATs
- Principal applications: Automotive, Power, Industrial

~80% market share as per TechInsights

- Installed base of ~820 systems
- Typical price: € 1~2 million per system
- ~5% of total Besi revenue

80% revenue from Semiconductor markets / 20% from adjacent markets

Tin solder plating

EPL: leadframe tin solder plating system

- ~80% market share as per Tech Insights
- ~50% of Besi Plating revenues

Leading customers

ROHM SEMICONDUCTOR, life.augmented, ASE GROUP, NXP, UTAC, infineon, Amkor Technology, BPIL

Adjacent Markets:

Connectors, Solar and Foil plating

Besi Plating Growth Drivers

High-power modules require new plating solutions

- Mold Deflashing and adhesion promotion
- For use in EV drive trains, renewables, industrial, household and Integrated Power Modules

Automotive investment increasing

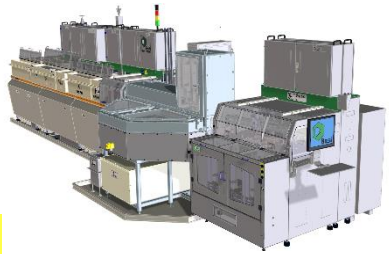
- More chips per car, both EV and ICE
- Increasing automotive quality requirements need more process steps / capital intensity

Increase value proposition to customers

- Implement sophisticated automated quality assurance on process chemistry
- Integrate robotics and software for highly automated production lines
- Reduce electrical and chemical consumption to enhance ESG characteristics

More Stringent Automotive Quality Demands Require Additional Wet Process Technologies

Chemical Deflash



Growth

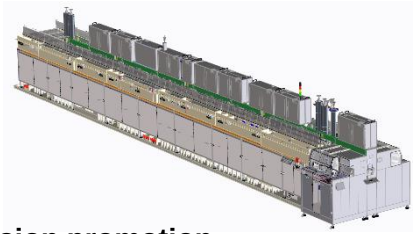
CDL:
- Mold deflashing without delamination

Flux cleaning

New

Flux cleaning:
- Removal of flux, after clip attach

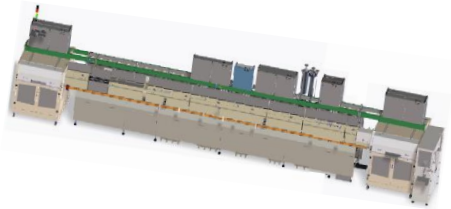
Mold adhesion



Growth

Mold adhesion promotion:
- Improve ‘sticking’ of the mold compound

Wettable flank



New

WFL:
Wettable flank tin plating of QFN’s

VII. Q&A